Power Stamp; Controller Stamp Unit Specification

1\ Function and feature specification

This description defines the footprint and function of the standard PSA "CONTROLLER STAMP" power converter that is to be used in conjunction with the PSA "SATELLITE STAMP" power converter.

The function of this power converter is to extend the power and current rating of the standard PSA family of products.

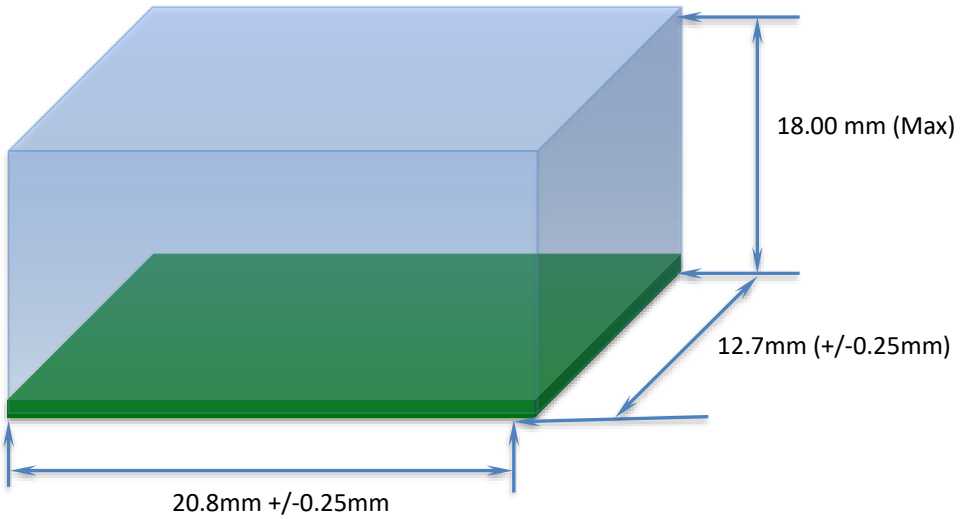
Parameter	Specification	Notes
Input voltage	54V nominal (36Vdc to 60Vdc)	Input to be <ELV limit
Output voltage	4.75V to 13.2V (*)	Supply voltage for VDD at the satellite(s)
Output current	Supplying up to 6 satellites (*)	Supply current for VDD at the satellite(s)
Output voltage	4.5V to 5.5V (*)	Supply voltage for VCTRL VCC at the satellite(s)
Output current	Supplying up to 6 satellites (*)	Supply current for VCTRL VCC at the satellite(s)
Control	PMBus (*)	Industry standard command set
	AVSBus or SVID control (*)	Exclusively one or other control function.
	Sense/Enable function	
Address	PMBus address	Address definitions as listed in this document.

(*) refer to each member's official documentation for consolidated specifications

2\ Power-stamp Controller Stamp envelope dimensions.

Power Stamps are defined by the maximum outer envelope dimensions. The length and width are defined and are fixed dimensions. The height defined is the maximum height allowable for designs which may not use the maximum available space.

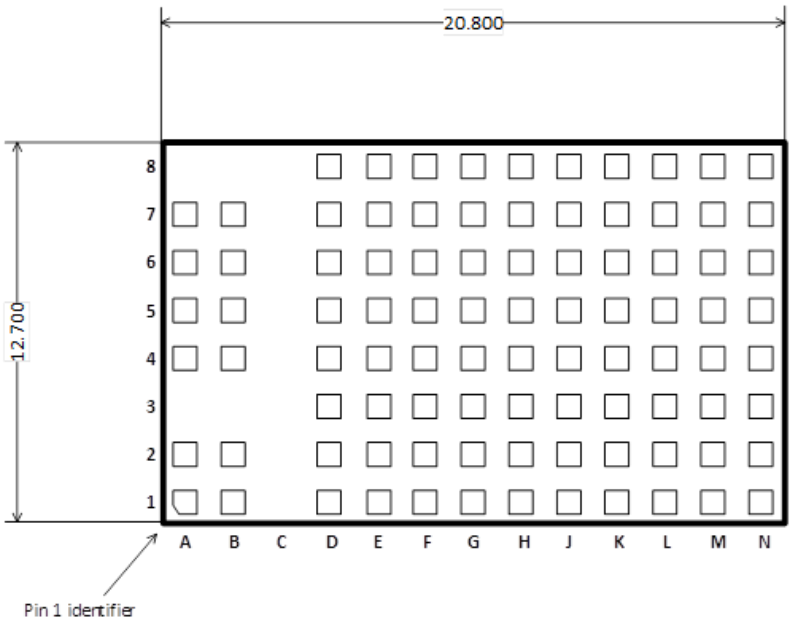
The "Controller Stamp" is described as;



3\ Interconnect details

3.1\ Pad locations for the PSA Controller Stamp.

Top view of the module with pad locations and names shown



TOP VIEW THROUGH THE PRODUCT

3.2\ Signal Pad function description for the PSA CONTROLLER STAMP module;

The signal pad connections available from the Controller Stamp are shown below (bottom view of the Controller Stamp)

	A	B	C	D	E	F	G	H	J	K	L	M	N	
1	+IN	+IN		TMP5	PUCDTO	PUCDTI	PUCCS	PUCCK	PWM3Y	PWM4Y	PWM5Y	PWM2Y	PWM2X	1
2	+IN	+IN		TMP3	CSP5	CSN5	PWM1X	PWM1Y	PWM3X	PWM4X	PWM5X	START5	GND	2
3				TMP1	CSP3	CSN3	GND	GND	GND	GND	PWM6X	START3	VCTRL	3
4	-IN	-IN		TMP2	CSP1	CSN1	GND	GND	GND	GND	PWM6Y	START1	VCC	4
5	-IN	-IN		TMP4	CSP2	CSN2	GND	GND	GND	GND	VR_RDY	START2	VCC	5
6	VDD	EN_PRI#		TMP6	CSP4	CSN4	GND	GND	GND	GND	EN	START4	GND	6
7	VDD	RSVD NC		TMN	CSP6	CSN6	SALERT	SDA	SVDAT / AVSMDAT	VR_HOT#	VCCIO_OK	START6	PFAULT _IN#	7
8				VS_MON	VIN_MON	+S	-S	SADDR	SCL	SVCLK / AVSCLK	SV_ALRT / AVSSDAT	PIN_ALE RT#	FAULT#	8
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Table of Signal pads and descriptions

Pad #	Pad name	Pad Function	Pad #	Pad name	Pad Function
Pad A1	+In	+ve Input voltage	**Pad A4**	-In	-ve Input voltage
Pad B1	+In	+ve Input voltage	**Pad B4**	-In	-ve Input voltage
Pad C1	N/A	No Pad present	**Pad C4**	N/A	No Pad present
Pad D1	TMP5	Temperature sense Satellite 5	**Pad D4**	TMP2	Temperature sense Satellite 2
Pad E1	PUCDTO	Primary side microcontroller data O/P	**Pad E4**	CSP1	Current sense +ve Satellite 1
Pad F1	PUCDTI	Primary side microcontroller data input	**Pad F4**	CSN1	Current sense -ve Satellite 1
Pad G1	PUCCS	Primary side microcontroller chip-select	**Pad G4**	GND	Secondary side ground
Pad H1	PUCCK	Primary side u-controller clk	**Pad H4**	GND	Secondary side ground
Pad J1	PWM3Y	PWM signal for Satellite 3	**Pad J4**	GND	Secondary side ground
Pad K1	PWM4Y	PWM signal for Satellite 4	**Pad K4**	GND	Secondary side ground
Pad L1	PWM5Y	PWM signal for Satellite 5	**Pad L4**	PWM6Y	PWM signal for Satellite 6
Pad M1	PWM2Y	PWM signal for Satellite 2	**Pad M4**	START1	Start for Satellite 1
Pad N1	PWM2X	PWM signal for Satellite 2	**Pad N4**	VCC	Secondary side bias voltage
Pad A2	+In	+ve Input voltage	**Pad A5**	-In	-ve Input voltage
Pad B2	+In	+ve Input voltage	**Pad B5**	-In	-ve Input voltage
Pad C2	N/A	No Pad present	**Pad C5**	N/A	No Pad present
Pad D2	TMP3	Temperature sense Satellite 3	**Pad D5**	TMP4	Temperature sense Satellite 4
Pad E2	CSP5	Current sense +ve Satellite 5	**Pad E5**	CSP2	Current sense +ve Satellite 2
Pad F2	CSN5	Current sense -ve Satellite 5	**Pad F5**	CSN2	Current sense -ve Satellite 2
Pad G2	PWM1X	PWM signal for Satellite 1	**Pad G5**	GND	Secondary side ground
Pad H2	PWM1Y	PWM signal for Satellite 1	**Pad H5**	GND	Secondary side ground
Pad J2	PWM3X	PWM signal for Satellite 3	**Pad J5**	GND	Secondary side ground
Pad K2	PWM4X	PWM signal for Satellite 4	**Pad K5**	GND	Secondary side ground
Pad L2	PWM5X	PWM signal for Satellite 5	**Pad L5**	VR_RDY	Voltage regulator ready signal
Pad M2	START5	Start for Satellite 5	**Pad M5**	START2	Start for Satellite 2
Pad N2	GND	Secondary side ground	**Pad N5**	VCC	Secondary side bias voltage (G)
Pad A3	N/A	No Pad present	**Pad A6**	VDD	Primary side bias voltage
Pad B3	N/A	No Pad present	**Pad B6**	EN_PRI#	Primary side enable
Pad C3	N/A	No Pad present	**Pad C6**	N/A	No Pad present
Pad D3	TMP1	Temperature sense Satellite 1	**Pad D6**	TMP6	Temperature sense Satellite 6
Pad E3	CSP3	Current sense +ve Satellite 3	**Pad E6**	CSP4	Current sense +ve Satellite 4
Pad F3	CSN3	Current sense -ve Satellite 3	**Pad F6**	CSN4	Current sense -ve Satellite 4
Pad G3	GND	Secondary side ground	**Pad G6**	GND	Secondary side ground
Pad H3	GND	Secondary side ground	**Pad H6**	GND	Secondary side ground
Pad J3	GND	Secondary side ground	**Pad J6**	GND	Secondary side ground
Pad K3	GND	Secondary side ground	**Pad K6**	GND	Secondary side ground
Pad L3	PWM6X	PWM signal for Satellite 6	**Pad L6**	EN	Enable Pad
Pad M3	START3	Start for Satellite 3	**Pad M6**	START4	Start for Satellite 4
Pad N3	VCTRL VCC	Controller supply voltage VCC (G)	**Pad N6**	GND	Secondary side ground

Pad A7	VDD	Primary side bias voltage	**Pad A8**	N/A	No Pad present
Pad B7	RSVD N/C	Reserved pad (not connected)	**Pad B8**	N/A	No Pad present
Pad C7	N/A	No Pad present	**Pad C8**	N/A	No Pad present
Pad D7	TMN	Temp sense -ve common for TMN of all Satellites.	**Pad D8**	VSRMON	+In voltage monitor – Input for the controller (G)
Pad E7	CSP6	Current sense +ve Satellite 6	**Pad E8**	VIN_MON	+In voltage monitor – Output from the aux converter
Pad F7	CSN6	Current sense -ve Satellite 6	**Pad F8**	+S	Remote sense +ve
Pad G7	SALERT#	PMBus Alert (active low)	**Pad G8**	-S	Remote sense -ve
Pad H7	SDA	PMBus data	**Pad H8**	SADDR	PMBus address setting
Pad J7	SVDAT / AVSMDAT	SVID data / AVS MData	**Pad J8**	SCL	PMBus clock
Pad K7	VR_HOT#	SVI VR hot	**Pad K8**	SVCLK / AVSCLK	SVID clock / AVS clock
Pad L7	VCCIO_OK	VCC fault shutdown – immediate unit shutdown	**Pad L8**	SVALRT / AVSSDAT	SVID alert / AVS SData
Pad M7	START6	Start for Satellite 6	**Pad M8**	PIN_ALERT#	SVI Pin Alert #
Pad N7	PFAULT_IN#	Primary side fault indicator	**Pad N8**	FAULT#	Programable fault indicator

Notes;

a\ The areas for 0V connection through the centre line of the module.

b\ The relative grouping of similar signals (by colour in the grid-matrix above)

c\ The grouping of -In and GND pads

d\ All CSP* and CSN*; When not used CSxP should be shorted to CSxN and then to Vout.

e\ PM_ADDR; May have a local pull-down resistor to GND

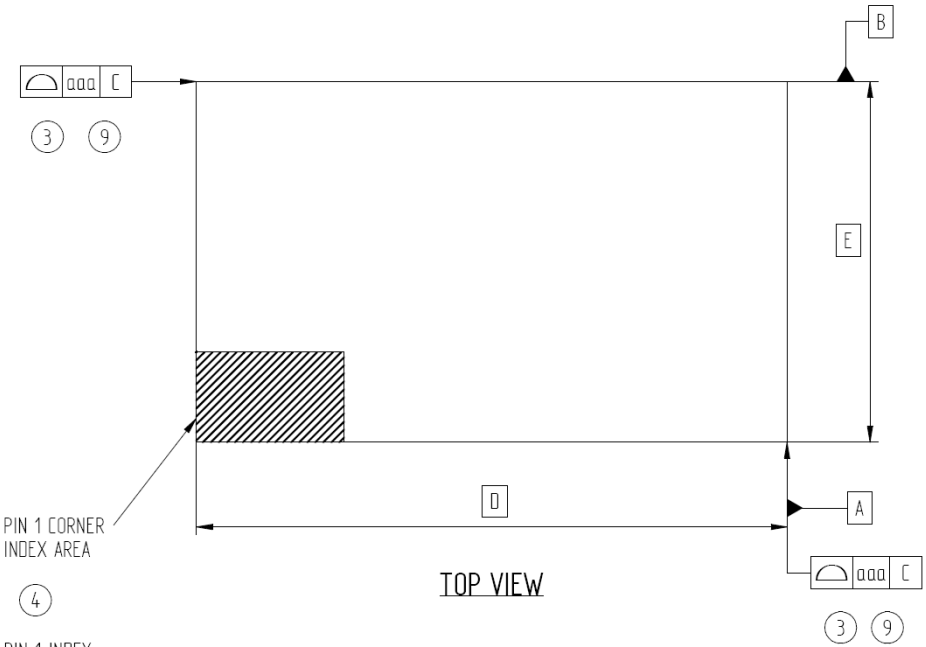
f\ SDA and SCL; Should have a pull-up resistor to either 3.3V or 5V

g\ See section 5.1 for the descriptions for the connections to the controller stamp in an application.

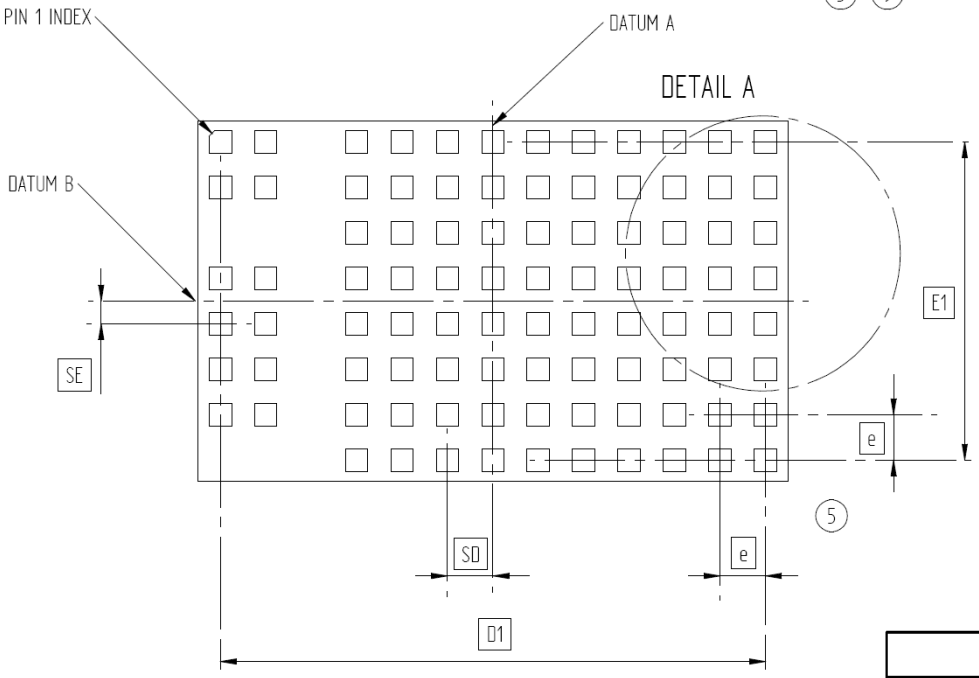
h\ See section 9.7 for EN / VCCIO_OK further details

4\ Mechanical drawings

4.1\ The diagram below shows the centre points of the PAD location and PAD size required to host the Controller Stamp



TOP VIEW



BOTTOM VIEW

DIMENSION VARIATIONS	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.15
eee	0.15
fff	0.08

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
D	-	20.80	-
E	-	12.70	-
D1		19.20	
E1		11.20 BSC	
e		1.60 BSC	
MD	-	13	-
ME	-	8	-
n	-	92	-
SD	-	1.60	-
SE	-	0.80	-

Notes;

1\ Footprint compliant to IPC7351C and JEDEC JEP95 – DG 4.25, SPP-010, Issue B

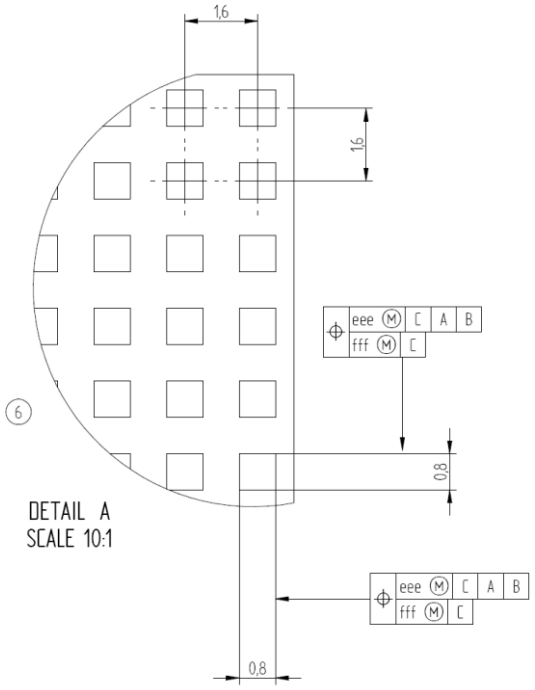
2\ Footprint compliant to IPC9592-B guidance;

- Primary positive input to 0V clearance dependant on the implementation of an input fuse and application insulation test
- Primary to secondary; basic insulation provided by footprint. Functional or Basic insulation within the Power Stamp will be dependent on the respective Power Stamp being considered.

3\ Zero Orientation with Pad 1 in Lower Left Corner of footprint; compliant to IEC 61188-7 and IPC-7351C “Level B”

4.2\ Termination specifications

Recommended PAD Size (in mm) and notes on the section 4.* drawings;

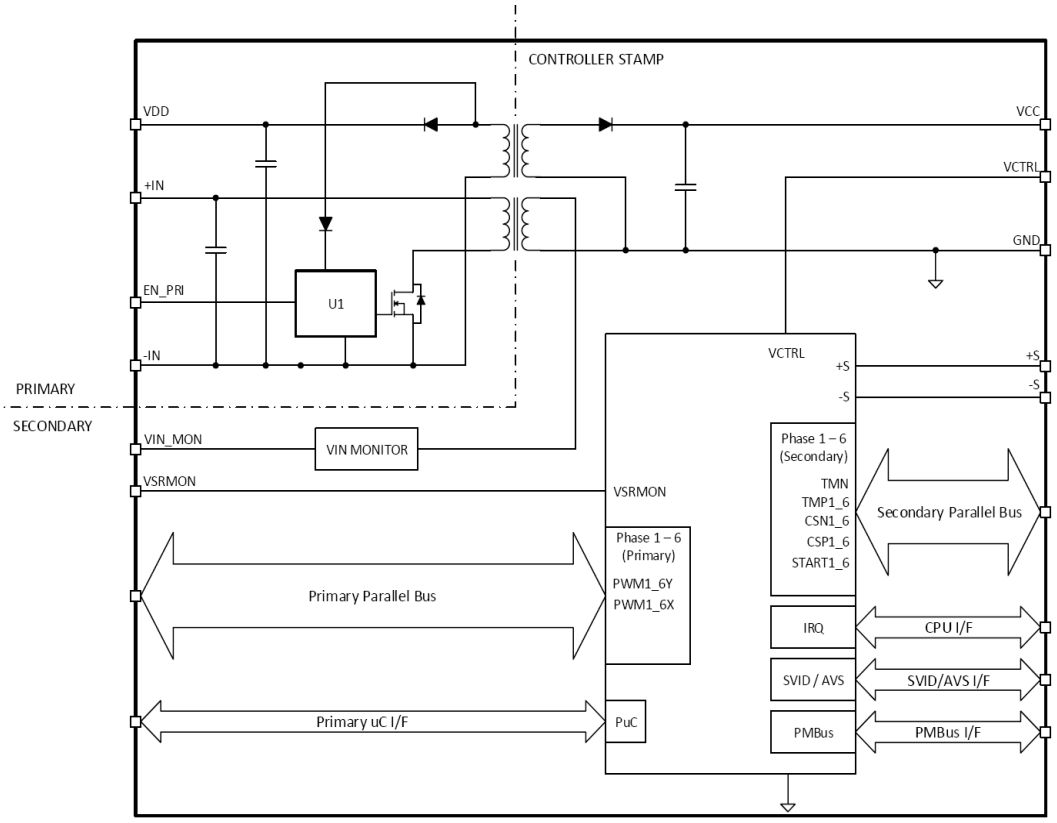


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DATUM "C" IS THE SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE PIN IDENTIFIER MAY BE EITHER A LABEL, A MARKED FEATURE OR A CHAMFERED EDGE
5. DIMENSION 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS
6. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION
7. BOTTOM VIEW OF TYPICAL MODULE PCB SHOWN FOR ILLUSTRATION PURPOSES ONLY
8. OVERALL MODULE HEIGHT NOT TO EXCEED 18mm
9. SEE INDIVIDUAL MODULE DATA SHEET FOR DETAILED TOP AND SIDE VIEW

5\ General information

The controller stamp is intended to provide all of the user-interface, control and supply voltage demands of up to 6 Power Stamp Satellites, thus enabling the power-conversion to be accomplished without any demands imposed on the host application.



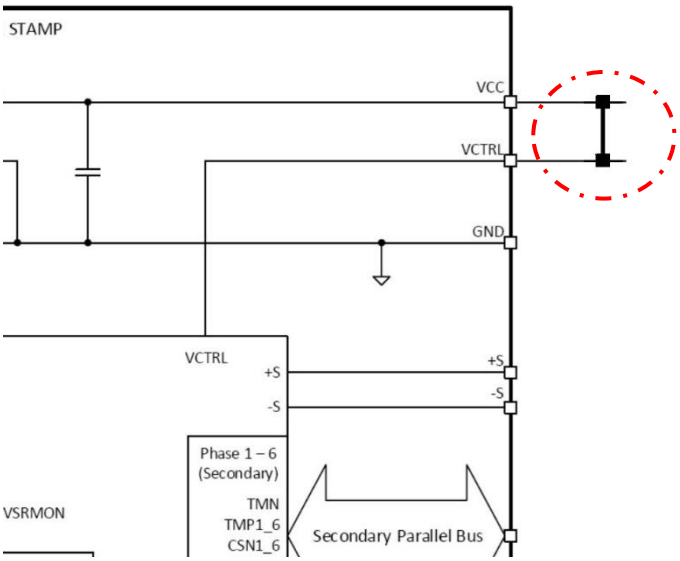
5.1\ Notes on control-stamp connections

5.1.1\ VCC and VCTRL connection

The VCC Pins are intended to supply all the Satellites Stamps connected to the Controller Stamp in the actual converter.

The VCTRL connection is the bias supply for the internal controller of the Controller Stamp and is not internally connected to VCC for testing and evaluation purposes.

In applications, it is necessary to place a zero-ohm link or to simply short the pins as shown below in the dotted line circle



5.1.2\ VSRMON connection

The VSRMON pin is intended to implement a precise input voltage monitor. In order to sense in the most precise manner the input voltage in the case of Isolated and non-Isolated applications the function is brought out separately from the controller stamp.

In the case of an Isolated topology, the pin can be shorted with VIN_MON which is providing information about the input voltage.

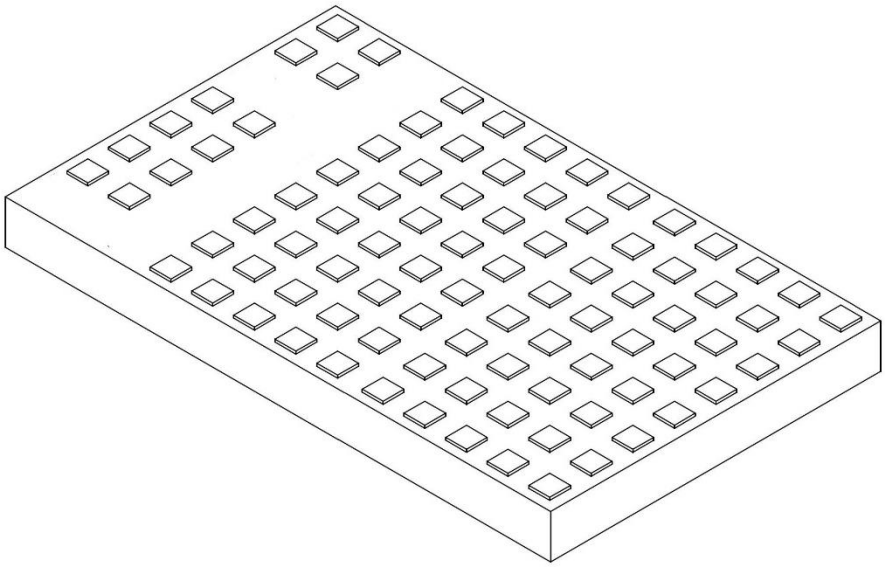
In the case of a non-isolated topology, the VSRMON pin can be directly tied to VIN through a proper resistor divider to implement a more accurate VIN sense functionality.

The VIN-Mon function has a function of a ratio of a 40:1 representation of the input voltage.

6\ Generic Controller stamp viewed from the bottom

The bottom side of the Controller Stamp PCB will appear to be as shown below, with a matrix of pads provided for all terminations.

.



7\ Module address setting.

The setting of the address of the module by resistor value is a standard function and is described as;

PSA Stamp addressing		Resistor_down (on the host board)		Resistor_UP (inside the Controller unit)	
7-Bit based address (SMBus)	8-bit Based address	Resistor series	Resistor value	Resistor series	Resistor value
0x5C	0xB8	E12	OPEN	E12	10,000
0x5A	0xB4	E12	220,000	E12	10,000
0x59	0xB2	E12	120,000	E12	10,000
0x58	0xB0	E12	82,000	E12	10,000
0x74	0xE8	E24	62,000	E12	10,000
0x72	0xE4	E96	48,700	E12	10,000
0x71	0xE2	E12	39,000	E12	10,000
0x70	0xE0	E12	33,000	E12	10,000
0x6C	0xD8	E48	27,400	E12	10,000
0x6A	0xD4	E48	23,700	E12	10,000
0x69	0xD2	E96	20,500	E12	10,000
0x68	0xD0	E48	17,800	E12	10,000
0x64	0xC8	E96	15,800	E12	10,000
0x62	0xC4	E96	13,700	E12	10,000

0x61	0xC2	E48	12,100	E12	10,000
0x60	0xC0	E96	10,700	E12	10,000

8\ Application Block Diagrams

8.1 Isolated block diagrams

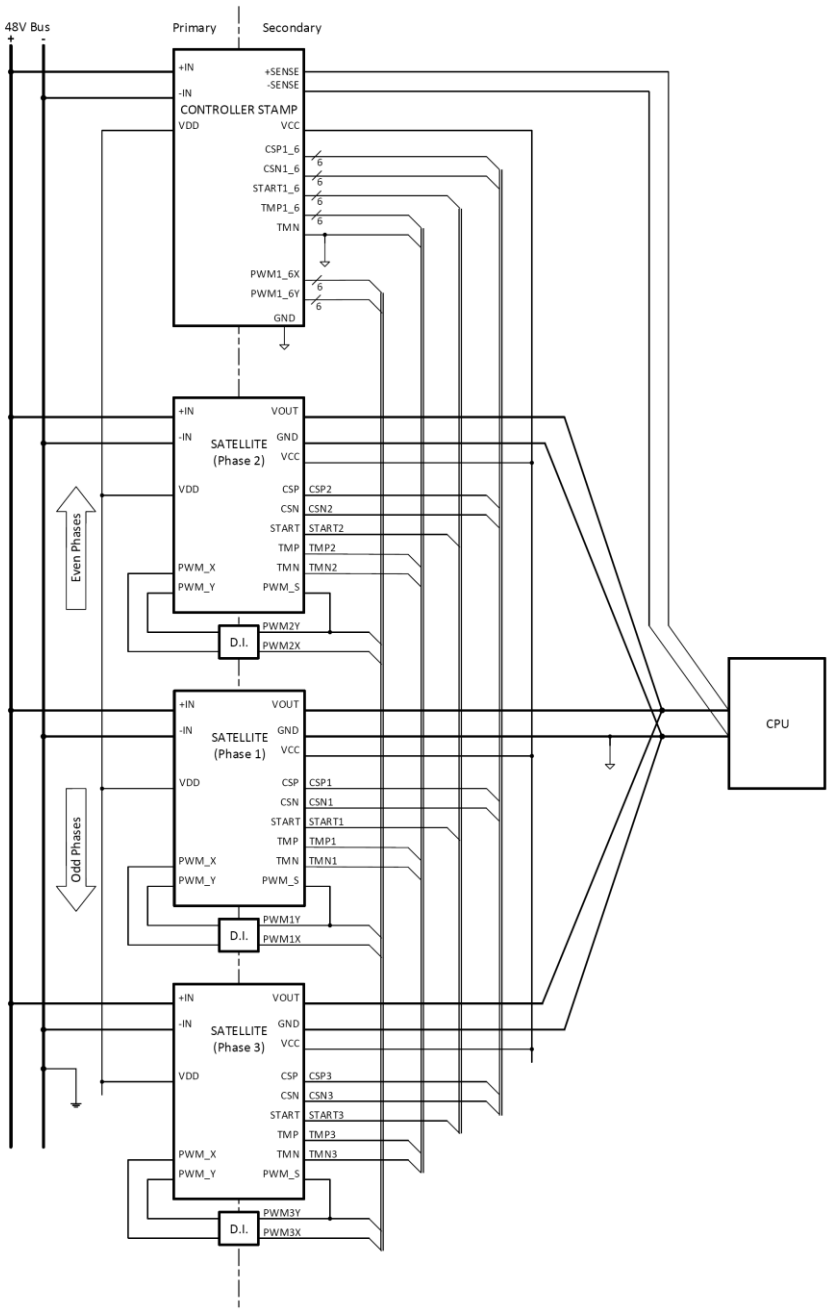
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamps (on the left),

or,

- The Controller Stamp plus Satellite Stamp configuration where the Controller incorporates the controller to control the satellites within itself.

The Power stages are isolated, and the isolation of the signals is provided by the function of the external digital isolator component shown as “D.I.” in the diagrams. (Note; The Digital isolator is shown as the isolation stage, not the actual component to be used in the application)



Isolated architecture with Controller-stamp + Satellites

8.2 NON-Isolated block diagrams

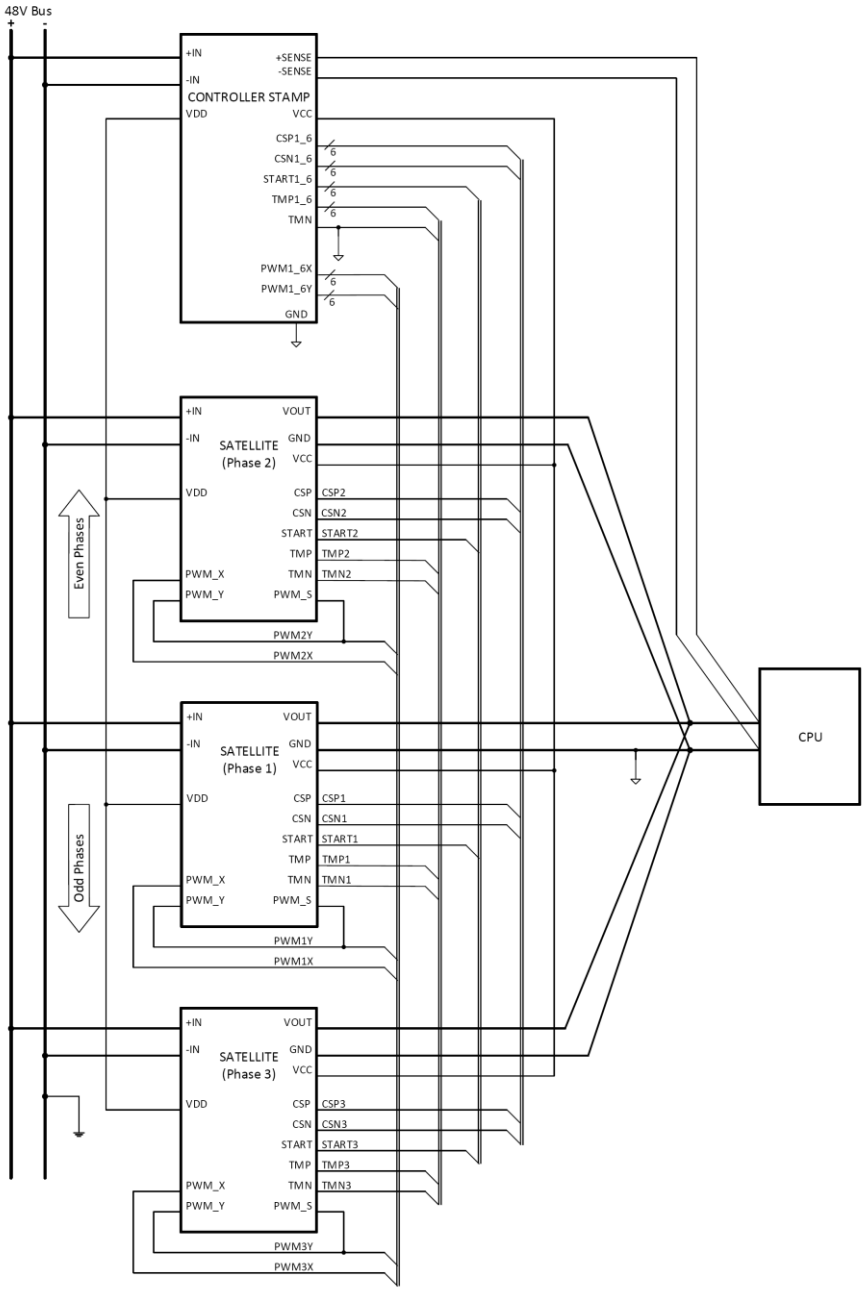
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamps (on the left),

or,

- The Controller Stamp plus Satellite Stamp configuration where the Controller incorporates the controller to control the salves within itself.

The Power stages are isolated, however, in this configuration the digital isolator component can be eliminated from the network.



Non-Isolated architecture with Controller-Stamp + Satellites

8.3 Relative phase locations

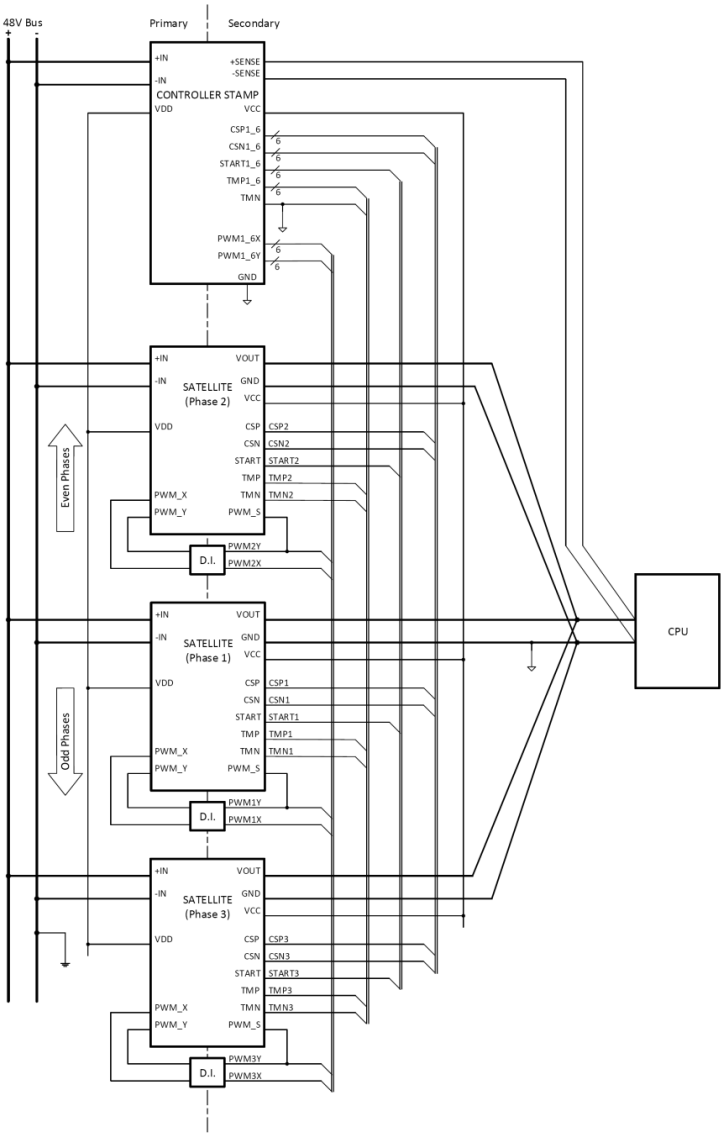
The diagrams show where the PSA recommend the sequential placement of the individual phases in relative terms to each other and the target load device. The rules are;

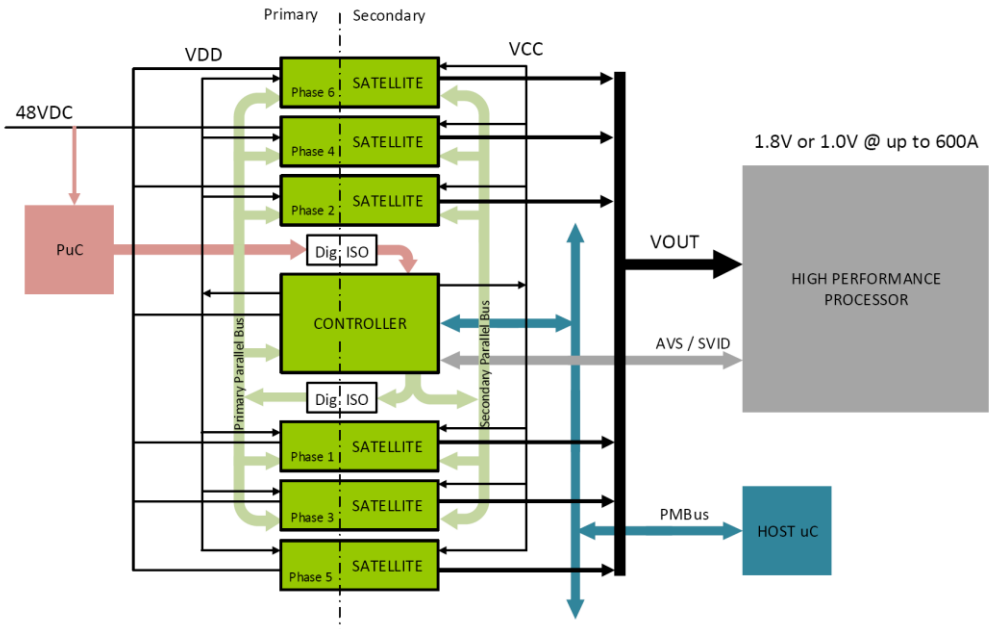
- To start from the centre
- To group odd and even phases

These 2 rules are recommended if phase-shedding is to be employed, and best possible control response of the network of converters can be achieved

The diagrams show examples of isolated networks of units with both an external controller, or Controller Stamp plus Satellite Stamp configuration.

(Note; The Digital isolator is shown as the isolation stage, not the actual component to be used in the application)





8.4\ Application Safety Standard compliance.

All applications require an appropriately selected protection element incorporated into the input path to each group or interconnected network of Power Stamps with single output voltage. I.e. each Power Stamp group or network must have a correctly selected fuse on its respective input.

The Power Stamp footprint complies to creepage and clearance distances as defined for functional insulation between V-in and 0V respectively and allows for functional or basic insulation between primary and secondary sides. Applications and designs where Power Stamps are used would be compliant to safety standards when the application has been tested to withstand electric strength tests for functional insulation as defined in the standards IEC60950 and IEC62368 respectively. I.e. when tested with a short-circuit applied within the application to simulate a single fault condition.

9\ Standard functions

9.1\ Voltage control

The PSA Controller Stamp is a multi-Satellite controller with a complete control logic and protections to realize a high-performance high-efficiency step-down DC-DC voltage regulator optimized for advanced microprocessor, memory and ASIC power supply with direct conversion from 48V bus.

The control loop is based upon the high performance Digital STVCOT™ which enables fast load transient response without suffering from a beating effect while maintaining a near constant switching frequency in a steady state allowing the minimization the output filter components.

The Controller Stamp reads the current information delivered from each of the Satellite Stamps. With this information, the Controller Stamp adjusts the control signals sent to the Satellites to equalize the average current carried by each stamp.

To guarantee the load-CPU's safety under all circumstances, a complete set of protection features are applied to output voltage/current, input voltage/current, feedback disconnection, temperature, input/output power and catastrophic failures.

Energy proportionality features modify the number of active Satellites to optimize the efficiency over the whole load range.

All the required parameters of both the control loop and power management features are programmable through dedicated PMBus™ commands

9.2\ Load shedding and Energy proportionality,

The PSA Controller Stamp is capable to support CPU-Link bus-driven power state command to improve the overall conversion efficiency by shedding Satellites and entering Pulse-Skip mode.

Reconfiguration through the PMBus™ means that these features can be enabled regardless of whether a command is issued through the CPU-bus (either SVI or AVS), thus allowing the optimization of the conversion efficiency in every instant of the operation of the Power Stamps.

Satellite Shedding allows the number of working Stamps to be adjusted and optimized according to the delivered current while still maintaining the benefits of the multi-cell regulation. The end user can program switch-over threshold current [in Amps] for every cell number transition, with hysteresis. Sleeping Satellites are reset in case of dynamic voltage transitions

9.3\ Output Voltage Positioning

Output voltage positioning is performed by programming the digital control loop parameters and (optional) droop function effect using the dedicated PMBus™ commands. The Controller Stamp embeds a remote-sense buffer to remotely sense the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated and compensates for board and connection losses. Keeping the sense traces parallel and guarded by a power plane results in the common mode coupling for any picked-up noise to be avoided.

The controller reads the current delivered by the additional Satellite units through the CSPx/CSNx pins generating an internal error, which is added to the remote buffer output causing the output voltage to vary accordingly thus implementing the desired load-line effect.

The output voltage setpoint can be configured to be programmed through PMBus™ (supporting standard commands such as VOUT_COMMAND, MARGIN, VOUT_MODE, etc..) or the high speed dedicated CPU link that can be further configured as SVI or AVS. The support of AVS or SVI is mutually exclusive and must be configured prior the unit to be turned enabled for regulation.

9.3.1 SVID control functions.

The PSA Controller Stamp is fully compliant with the Intel® VR13 PWM rev 1.6, document #544905 and the Intel® SVID protocol Rev1., document # 456098 within the limitations of VR13.HC. To guarantee proper interactions between VR and CPU, refer to these documents for bus design and layout guidelines. Different platforms may require different pull-up impedance on the CPUI-Link bus. Impedance matching and spacing must be followed. Refer to the PSA member own documentation for the list of supported features.

9.3.2 AVS Support

The PSA Controller Stamp is compliant with PMBus™ specification rev 1.3.1; 13 March 2015 – Part III related to the AVSBus support. Refer to this document for bus design and layout guidelines. Refer to the PSA member own documentation for the list of supported features.

The Controller Stamp Unit features a digital control technique: a fast analogue-to-digital converter (ADC) digitizes the error in the regulation. The resultant digital error signal is then fed into a digital PID compensator and then processed by the Digital STVCOT™ control logic generating the logic signals to drive the Satellite Stamps.

In the case of a high-performance digital load, it may be the case the control loop has to be designed for a controlled Output Impedance behaviour, typically in the range of the droop function load line programmed statically (DC). The bandwidth of the system has then to be designed in order to Control entertain the droop effect programmed in DC even over frequency, taking also in account the output capacitor bank mix and the board parasitic effects.

9.4\ PMBus command set

The PSA Controller Stamp is fully compliant with the PMBus™ specification part I and part II, revision 1.2 and with Part III, Revision 1.3.1 (www.pmbus.org). Controller Stamps are fully compatible with the PMBus™ specification for read/write access in the byte, word and block mode.

Refer to your PSA member own documentation for the full set of supported PMBus™ commands and features.

9.5\ Telemetry and Protections

The Controller Stamp Unit monitors input/output voltages, powers and current in order to manage OV, UV and OC events and to provide telemetry data to the CPU-link and PMBus™ interfaces. According to standard PMBus™ implementation, each protection features a programmable warning and fault limits and actions. Protections can additionally be configured to trigger special outputs such as FAULT pin and SM_ALERT# assertion.

Some of the variables monitored are directly monitored through dedicated ADC while others are computed starting from the available data. Any variable that is computed uses consistent data, i.e. data that refers to the same averaging period.

Refer to your PSA member own documentation for further details of telemetry and protection setting, accuracy and programmability

9.5.1 Black Box Recorder

The black box feature is aimed to picture precisely the status of the device at the fault occurrence. The device records the status of the configured flags before (OLD) and after (NEW) a fault event occurred and stores it into dedicated NVM sectors. The BBR picture is recorded into the device NVM and the information is preserved even in case of power cycling and/or re-trigger of the same protection. The dedicated reset command has to be issued to clear the BBR content.

9.6 Primary Enable function (Pri-EN#, pad B6)

The Primary Enable (Pri-EN) function of the control stamp is defined as “Negative enable” or “Active low”. This connection is to be pulled to 0V (or ground connection) to enable the unit. When left open-circuit this pad will float at “logic-high” via an internal pull-up function.

9.7 Enable function (En, pad L6)

The Enable (En) function of the control stamp will be defined as “positive enable” or “Active high” defined as;

- input high, rising >0.7Vdc
- input low falling <0.4Vdc

The EN pin is un-biased so it needs to be either pulled high or low – it cannot be left floating. The functionality of EN pin differs from VCCIO_OK (L7) that is aimed to sense VCCIO line in VR13HC application to implement a fast protection in case the VCCIO bias goes missing. VCCIO_OK must be shorted to VCC in case it is not used.

10\ Change History

This document is subject to change at any time pending the agreement of the founding membership of the PowerStamp Alliance**.**

Issue	Date	Issued by	Change
A	28th Nov 2019	A.Brown	- First revision
B	30th Jan 2019	R.Vai, A.Brown	- Modification to min I/P voltage to 36V (pg1) - Modification of power defined by the members (pg1) - Updated pin-out definition. - note added to block-diag info for DI stage.
C	5th Feb 2019	A.Brown	- Updated block diagram - Updated multi-stamp block diags. - Pin name change - VSRMON(In) to VS_MON - VIN_MON(out) to VIN_MON
D	5th Feb 2019	G. Mauri A.Brown	- Updated block diag
E	12th Feb 2019	G. Mauri A.Brown	- Updated block diagrams - Updated functional diagram - Updated module-phase location diagram
F	13th Feb 2019	R. Vai G. Mauri A.Brown	- Update to the Address table - Added the section 5.1 on the connections to the controller stamp. - Added mechanical outline and termination drawings.
1.0	6th Mar 2019	PSA Org	First public release
1.1	18th Sept 2019	A.Brown	Added VI-Mon function description to 5.1.2 Added section 9.6 for Primary-Enable function Added section 9.7 for enable function
1.2	18th Sept 2019	A.Brown	# added to Pri-En to be Pri-En#
1.3	June 2020	R. Vai	- Updated notes to Table of Signal pads and descriptions - Updated Module address setting Table specifying 7bit based address - Added section 9.6