Power Stamp; Main Stamp Unit Specification

1\ Function and feature specification

This description defines the footprint and function of the standard PSA "MAIN STAMP" power converter that is to be used in conjunction with the PSA "SATELLITE STAMP" power converter.

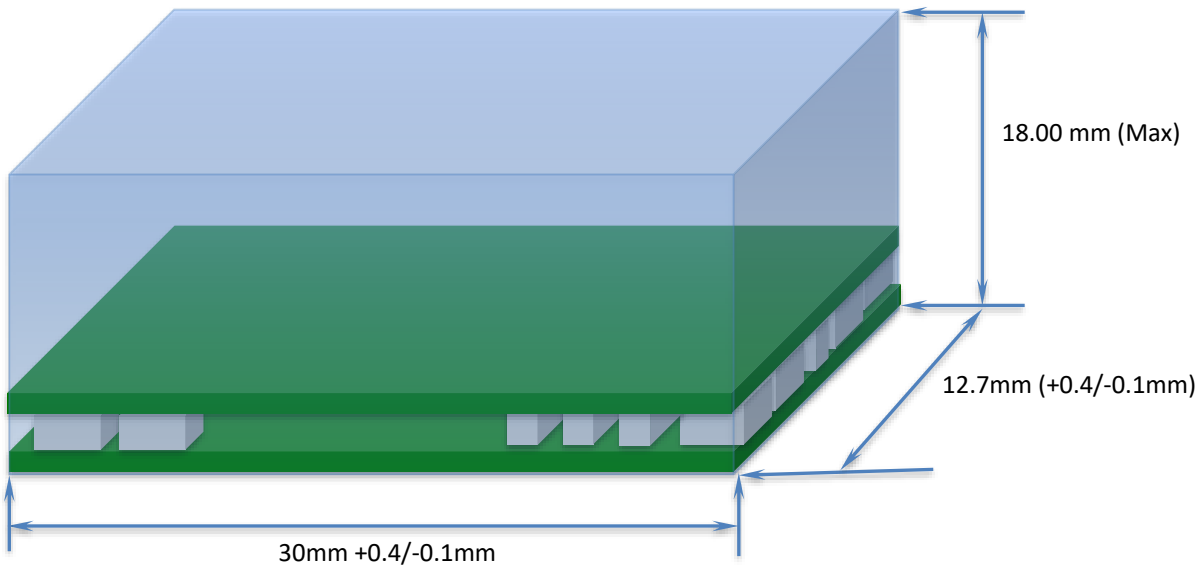
The function of this power converter is to extend the power and current rating of the standard PSA family of products.

Parameter	Specification	Notes
Input voltage	54V nominal (40Vdc to 60Vdc)	Input to be <ELV limit
Output voltage	0.5v to 2v5	
Output current	Up to 100A	Expansion stamp current rating
Control	PMBus	Industry standard command set
	AVSBus or SVID control	Exclusively one or other control function.
	Sense/enable function	
Address	PMBus address	Address definitions as listed in this document.

2\ Power-stamp Main Stamp envelope dimensions.

Power Stamps are defined by the maximum outer envelope dimensions. The length and width are defined and are fixed dimensions. The height defined is the maximum height allowable for designs which may not use the maximum available space.

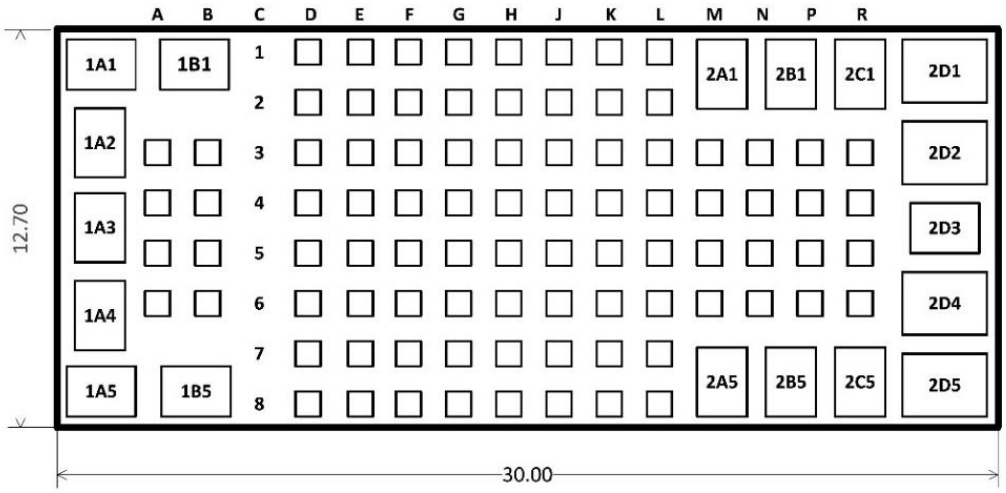
The "Main Stamp" is described as;



3\ Interconnect details

3.1\ Pad locations for the PSA Main Stamp.

Bottom view of the module with pad locations and names shown



3.2\ Power Pad function description for the PSA MAIN STAMP.

Short descriptions of the individual pads on the unit are;

Pad #	I/O	Pad name	Pad Function
1A1	I	+IN	Positive Input voltage supply connection. Connect with appropriately sized PCB traces to input power supply and filter locally according to the load performances.
1A2	I	PWM_Y	PWM input Y connection. Connect with PWM1Y (PAD G1) output directly or use digital isolator in case of isolated topologies.
1A3	I	VDD	Primary Auxiliary voltage supply. Connect to external 5V bias for correct operation.
1A4	I	PWM_X	PWM input X connection. Connect with PWM1X (PAD G2) output directly or use digital isolator in case of isolated topologies.
1A5	I	+IN	Positive input voltage supply connection. Connect with appropriately sized PCB traces to input power supply and filter locally according to the load performances.
1B1	n/a	-IN	Primary side ground connection. Connect with PCB primary-side GND power plane.
1B5	n/a	-IN	Primary side ground connection. Connect with PCB primary-side GND power plane.
2A1	n/a	No connection	Pad present, no connection made.
2A5	n/a	No connection	Pad present, no connection made.

Pad #	I/O	Pad name	Pad Function
2B1	n/a	No connection	Pad present, no connection made.
2B5	I	VCC	Secondary side Auxiliary voltage supply, connect to external 5V bias.
2C1	n/a	No connection	Pad present, no connection made.
2C5	n/a	No connection	Pad present, no connection made.
2D1	n/a	GND	Secondary side ground connection. Connect with PCB GND power plane.
2D2	O	VOUT	Positive output voltage connection. Connect with appropriately sized PCB traces to the output load.
2D3	n/a	No connection	Pad present, no connection made.
2D4	O	VOUT	Positive output voltage connection. Connect with appropriately sized PCB traces to the output load.
2D5	n/a	GND	Secondary side ground connection. Connect with PCB GND power plane.

3.3\ Signal Pad function description for the PSA MAIN STAMP module;

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	N/A	N/A	N/A	PFAULT_IN#	PUC DTO	PUCDTI	PWM 1Y	PWM 2Y	PWM 3Y	PWM 4Y	PWM 5Y	N/A	N/A	N/A	N/A	1
2	N/A	N/A	N/A	VSR MON	PUCCS	PUCCK	PWM 1X	PWM 2X	PWM 3X	PWM 4X	PWM 5X	N/A	N/A	N/A	N/A	2
3	-IN	-IN	N/A	TMP5	CSP5	CSN5	GND	GND	GND	GND	PWM 6X	PWM 6Y	START5	GND	GND	3
4	-IN	-IN	N/A	TMP3	CSP3	CSN3	GND	GND	GND	GND	FAULT#	START6	START3	GND	GND	4
5	-IN	-IN	N/A	TMP2	CSP2	CSN2	GND	GND	GND	GND	VR_RDY	VREG	START2	GND	GND	5
6	-IN	-IN	N/A	TMP4	CSP4	CSN4	GND	GND	GND	GND	EN	VCTRL	START4	GND	GND	6
7	N/A	N/A	N/A	TMP6	CSP6	CSN6	SALERT	SDA	SVDAT / AVSMDAT	VR_HOT#	VCCIO_OK	N/A	N/A	N/A	N/A	7
8	N/A	N/A	N/A	TMN	+S	-S	SADDR	SCL	SVCLK / AVSCLK	SVALRT / AVSSDAT	PAD_ALERT#	N/A	N/A	N/A	N/A	8
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

The signal pad connections available from the Main Stamp are shown below

Notes;

a\ The areas for 0V connection through the centre line of the module.

b\ The relative grouping of similar signals (by colour in the grid-matrix above)

c\ The grouping of -In and GND pads

d\ The grid above does NOT include the power connections

Table of Signal pads and descriptions

Pad #	Pad name	I/O	Pad Function
A1	N/A	n/a	No Pad present
A2	N/A	n/a	No Pad present
A3	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
A4	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
A5	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
A6	N/C (-Vin)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
A7	N/A	n/a	No Pad present
A8	N/A	n/a	No Pad present
B1	N/A	n/a	No Pad present
B2	N/A	n/a	No Pad present
B3	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
B4	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
B5	N/C (-In)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
B6	N/C (-Vin)	n/a	Pad present, N/C, Thermal via. Connect to primary-side GND for thermal purposes only.
B7	N/A	n/a	No Pad present
B8	N/A	n/a	No Pad present
C1	N/A	n/a	No Pad present
C2	N/A	n/a	No Pad present
C3	N/A	n/a	No Pad present
C4	N/A	n/a	No Pad present
C5	N/A	n/a	No Pad present
C6	N/A	n/a	No Pad present
C7	N/A	n/a	No Pad present
C8	N/A	n/a	No Pad present
D1	PFAULT_IN#	I	Primary side fault indicator Input to stop operation in case a fault is detected in the primary side. Active Low.
D2	VSRMON	I	Feed-forward sensor input, Should have a local pull down resistor (Option to be in parallel with a capacitor) to GND, also connected to Vin via a resistor in non-isolated applications.
D3	TMP5	I	Temperature sense Satellite 5 Input. Connect with related Satellite TMP output pin in kelvin connection with its TMN output pin.

Pad #	Pad name	I/O	Pad Function
D4	TMP3	I	Temperature sense Satellite 3 Input. Connect with related Satellite TMP output pin in kelvin connection with its TMN output pin.
D5	TMP2	I	Temperature sense Satellite 2 Input. Connect with related Satellite TMP output pin in kelvin connection with its TMN output pin.
D6	TMP4	I	Temperature sense Satellite 4 Iinput. Connect with related Satellite TMP output pin in kelvin connection with its TMN output pin.
D7	TMP6	I	Temperature sense Satellite 6 Input. Connect with related Satellite TMP output pin in kelvin connection with its TMN output pin.
D8	TMN	I	Temp sense common for TMN of all Satellites. Star connection for all the satellite TMN outputs.
E1	PUCDTO	O	Primary side microcontroller data output
E2	PUCCS	O	Primary side microcontroller chip-select
E3	CSP5	I	Current sense +ve Satellite 5. Connect to Satellite 5 CSP output in kelvin connection with CSN pad. Short to VOUT when not used.
E4	CSP3	I	Current sense +ve Satellite 3. Connect to Satellite 3 CSP output in kelvin connection with CSN pad. Short to VOUT when not used.
E5	CSP2	I	Current sense +ve Satellite 2. Connect to Satellite 2 CSP output in kelvin connection with CSN pad. Short to VOUT when not used.
E6	CSP4	I	Current sense +ve Satellite 4. Connect to Satellite 4 CSP output in kelvin connection with CSN pad. Short to VOUT when not used.
E7	CSP6	I	Current sense +ve Satellite 6. Connect to Satellite 6 CSP output in kelvin connection with CSN pad. Short to VOUT when not used.
E8	+S	I	Remote sense +ve. Connect in kelvin pair with -S (pad F8) to the regulation point for VOUT.
F1	PUCDTI	I	Primary side microcontroller data input
F2	PUCCK	O	Primary side u-controller clk
F3	CSN5	I	Current sense -ve Satellite 5. Connect to Satellite 5 CSP output in kelvin connection with CSP pad. Short to VOUT when not used.
F4	CSN3	I	Current sense -ve Satellite 3. Connect to Satellite 3 CSP output in kelvin connection with CSP pad. Short to VOUT when not used.

Pad #	Pad name	I/O	Pad Function
F5	CSN2	I	Current sense -ve Satellite 2. Connect to Satellite 2 CSP output in kelvin connection with CSP pad. Short to VOUT when not used.
F6	CSN4	I	Current sense -ve Satellite 4. Connect to Satellite 4 CSP output in kelvin connection with CSP pad. Short to VOUT when not used.
F7	CSN6	I	Current sense -ve Satellite 6. Connect to Satellite 6 CSP output in kelvin connection with CSP pad. Short to VOUT when not used.
F8	-S	I	Remote sense -ve. Connect in kelvin pair with +S (pad E8) to the regulation point for VOUT.
G1	PWM1Y	O	PWM signal for Satellite 1 (Main). Connect directly to pad 1A2 (PWM_Y) in case of non isolated applications or through a digital isolator in case of isolated applications.
G2	PWM1X	O	PWM signal for Satellite 1 (Main). Connect directly to pad 1A4 (PWM_X) in case of non isolated applications or through a digital isolator in case of isolated applications.
G3	GND	n/a	Secondary side ground
G4	GND	n/a	Secondary side ground
G5	GND	n/a	Secondary side ground
G6	GND	n/a	Secondary side ground
G7	SALERT#	O	PMBus Alert (active low)
G8	SADDR	I	PMBus address setting. Connect a single resistor to GND to define the interface's address.
H1	PWM2Y	O	PWM signal for Satellite 2. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
H2	PWM2X	O	PWM signal for Satellite 2. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
H3	GND	n/a	Secondary side ground
H4	GND	n/a	Secondary side ground
H5	GND	n/a	Secondary side ground
H6	GND	n/a	Secondary side ground
H7	SDA	I/O	PMBus data
H8	SCL	O	PMBus clock
J1	PWM3Y	O	PWM signal for Satellite 3. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.

Pad #	Pad name	I/O	Pad Function
J2	PWM3X	O	PWM signal for Satellite 3. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
J3	GND	n/a	Secondary side ground
J4	GND	n/a	Secondary side ground
J5	GND	n/a	Secondary side ground
J6	GND	n/a	Secondary side ground
J7	SVDAT / AVSMDAT	I/O	SVID data / AVS MData
J8	SVCLK / AVSCLK	O	SVID clock / AVS clock
K1	PWM4Y	O	PWM signal for Satellite 4. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
K2	PWM4X	O	PWM signal for Satellite 4. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
K3	GND	n/a	Secondary side ground
K4	GND	n/a	Secondary side ground
K5	GND	n/a	Secondary side ground
K6	GND	n/a	Secondary side ground
K7	VR_HOT#	O	SVI VR hot
K8	SVALRT / AVSSDAT	O	SVID alert / AVS SData
L1	PWM5Y	O	PWM signal for Satellite 5. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
L2	PWM5X	O	PWM signal for Satellite 5. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
L3	PWM6X	O	PWM signal for Satellite 6. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
L4	FAULT#	O	Programable fault indicator
L5	VR_RDY	O	Voltage regulator ready signal
L6	EN	I	Enable Pad
L7	VCCIO_OK	I	VCC fault shutdown – immediate unit shutdown
L8	PIN_ALERT#	O	SVI Pin Alert #
M1	N/A	n/a	No Pad present
M2	N/A	n/a	No Pad present
M3	PWM6Y	O	PWM signal for Satellite 6. Connect directly in case of non isolated applications or through a digital isolator in case of isolated applications.
M4	START6	O	Start for Satellite 6. Connect to Satellite's START pin.

Pad #	Pad name	I/O	Pad Function
M5	VREG		Optional regulator input
M6	VCTRL		Controller supply voltage
M7	N/A	n/a	No Pad present
M8	N/A	n/a	No Pad present
N1	N/A	n/a	No Pad present
N2	N/A	n/a	No Pad present
N3	START5	O	Start for Satellite 5. Connect to Satellite's START pin.
N4	START3	O	Start for Satellite 3. Connect to Satellite's START pin.
N5	START2	O	Start for Satellite 2. Connect to Satellite's START pin.
N6	START4	O	Start for Satellite 4. Connect to Satellite's START pin.
N7	N/A	n/a	No Pad present
N8	N/A	n/a	No Pad present
P1	N/A	n/a	No Pad present
P2	N/A	n/a	No Pad present
P3	GND	n/a	Secondary side ground
P4	GND	n/a	Secondary side ground
P5	GND	n/a	Secondary side ground
P6	GND	n/a	Secondary side ground
P7	N/A	n/a	No Pad present
P8	N/A	n/a	No Pad present
R1	N/A	n/a	No Pad present
R2	N/A	n/a	No Pad present
R3	GND	n/a	Secondary side ground
R4	GND	n/a	Secondary side ground
R5	GND	n/a	Secondary side ground
R6	GND	n/a	Secondary side ground
R7	N/A	n/a	No Pad present
R8	N/A	n/a	No Pad present

Notes

a\ VSRMON; should have a local pull down resistor (Option to be in parallel with a capacitor) to GND, also connected to Vin via a resistor in non-isolated applications.

b\ All CSP* and CSN*; When not used CSxP should be shorted to CSxN and then to Vout.

c\ SADDR; May have a local pull-down resistor to GND

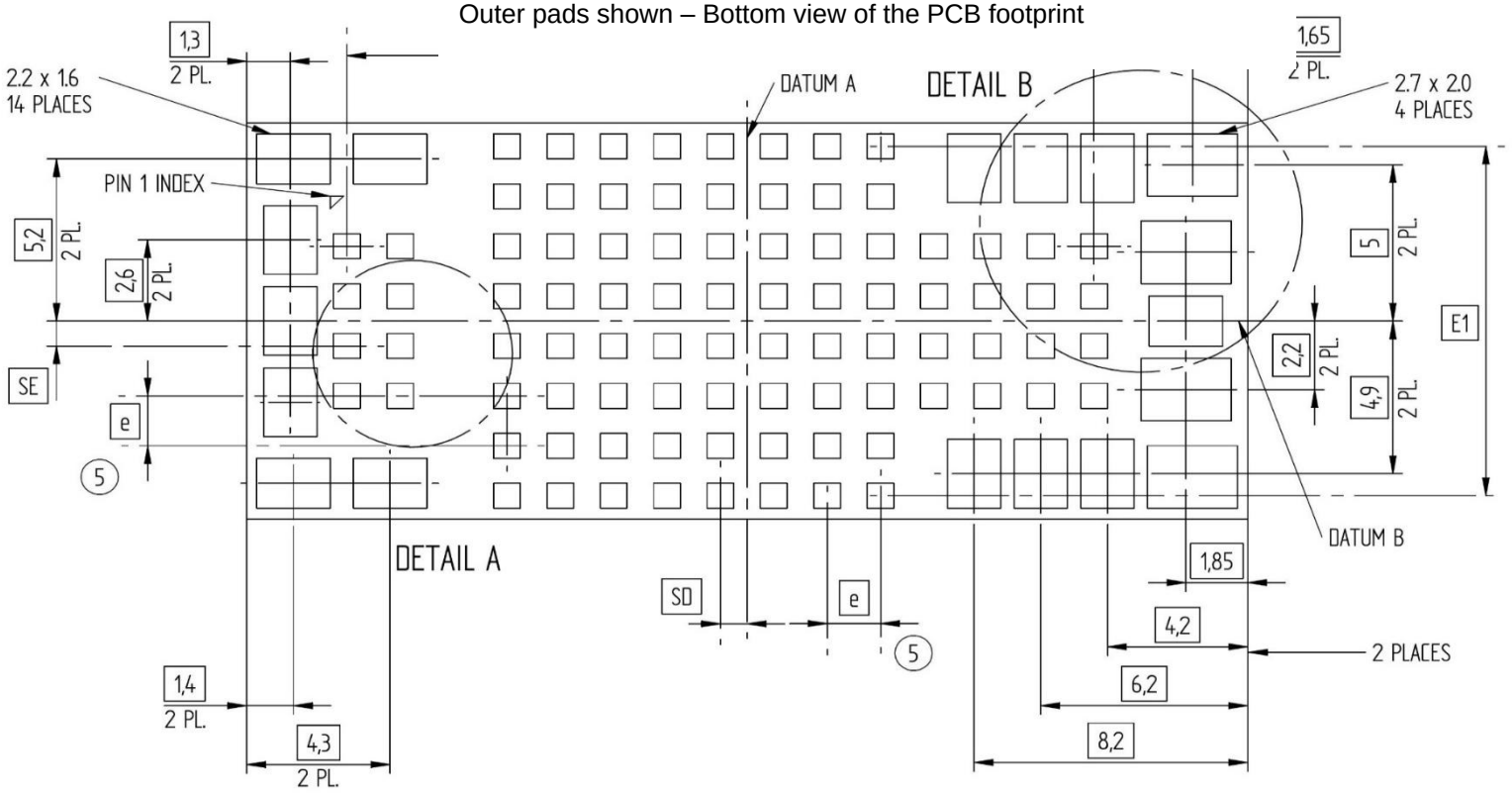
d\ SDA and SCL; Should have a pull-up resistor to either 3.3V or 5V

e\ See section 9.7 for EN / VCCIO_OK further details

4\ Mechanical drawings

4.1\ The diagram below shows the centre points of the PAD location and PAD size required to host the Main Stamp

Outer pads shown – Bottom view of the PCB footprint



Notes;

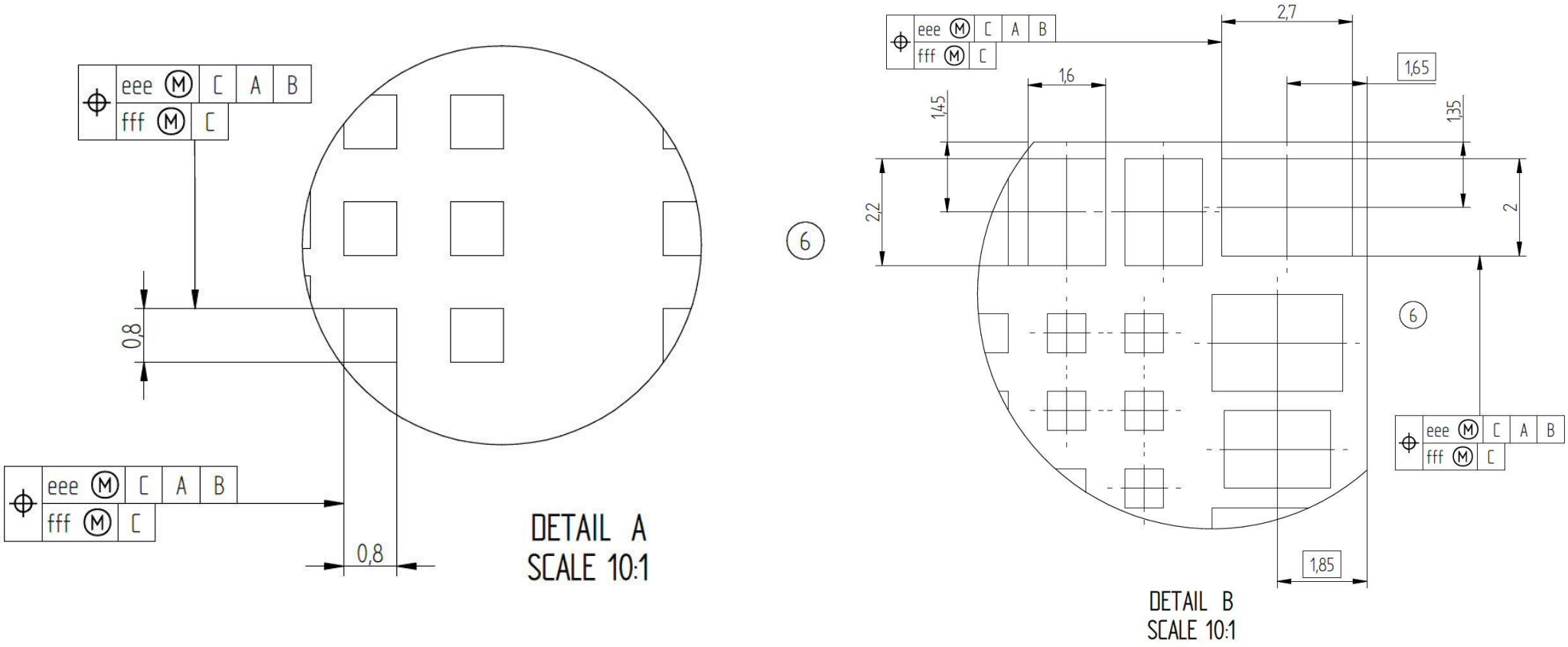
1\ Footprint compliant to IPC7351C and JEDEC JEP95 – DG 4.25, SPP-010, Issue B

2\ Footprint compliant to IPC9592-B guidance;

- Primary positive input to 0V clearance dependant on the implementation of an input fuse and application insulation test
- Primary to secondary; basic insulation provided by footprint. Functional or Basic insulation within the Power Stamp will be dependent on the respective Power Stamp being considered.

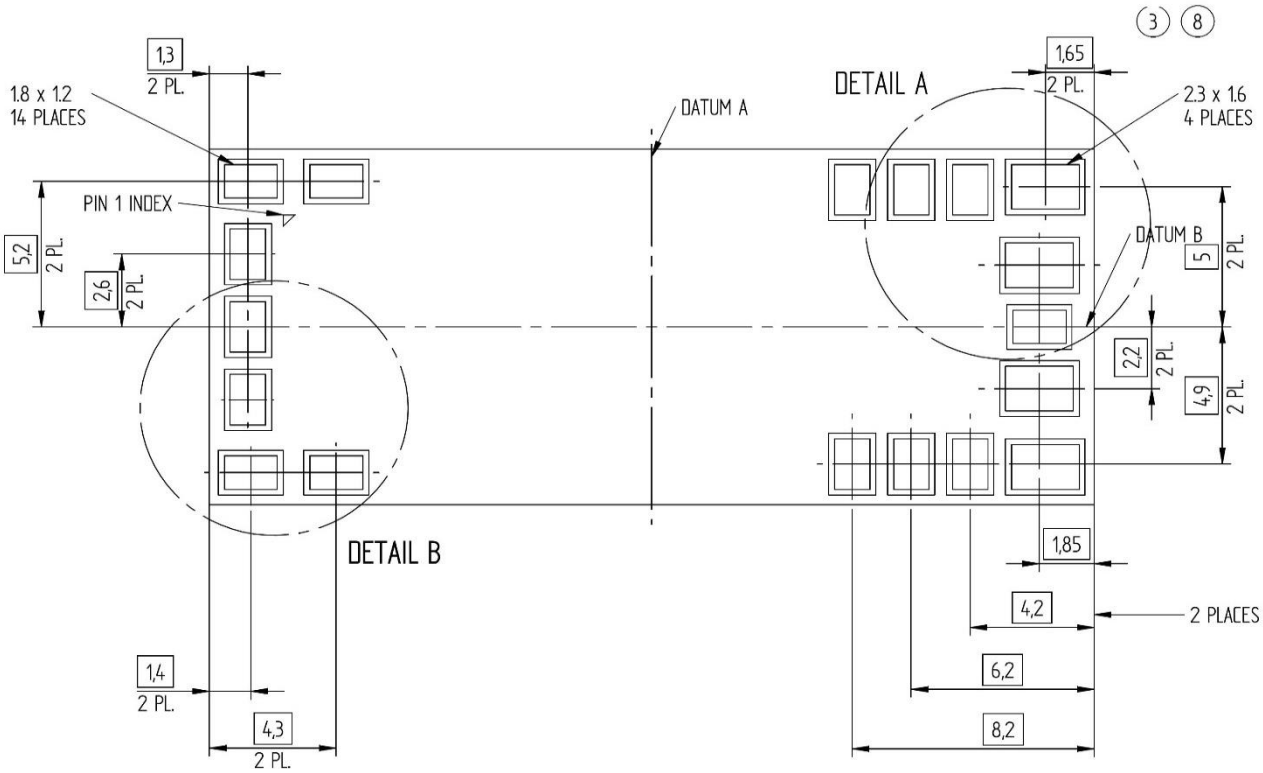
3\ Zero Orientation with Pad 1 in Lower Left Corner of footprint; compliant to IEC 61188-7 and IPC-7351C “Level B”

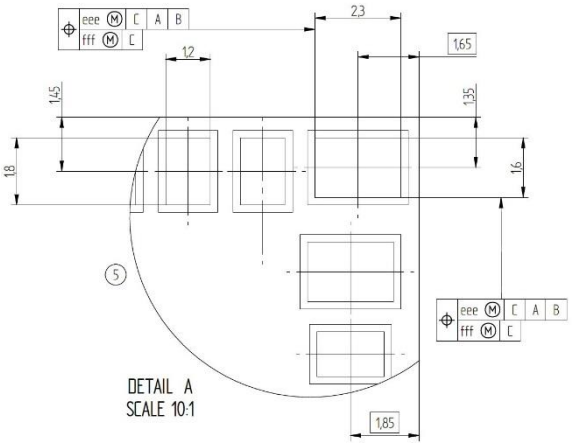
Additional detail information from the previous diagram

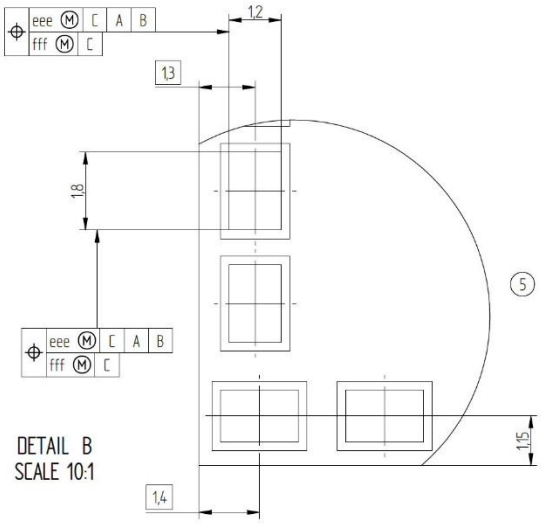


4.2\ Bottom view of the unit

Power pad termination shown (from the bottom side of the unit)







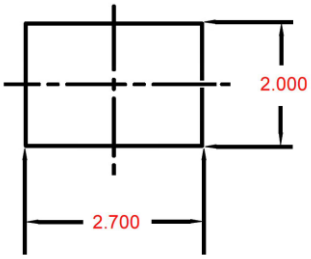
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DATUM "C" IS THE SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE PIN IDENTIFIER MAY BE EITHER A LABEL, A MARKED FEATURE OR A CHAMFERED EDGE
5. DIMENSION 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS
6. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION
7. BOTTOM VIEW OF TYPICAL MODULE PCB SHOWN FOR ILLUSTRATION PURPOSES ONLY
8. OVERALL MODULE HEIGHT NOT TO EXCEED 18mm
9. SEE INDIVIDUAL MODULE DATA SHEET FOR DETAILED TOP AND SIDE VIEW

DIMENSION VARIATIONS	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.15
eee	0.15
fff	0.08

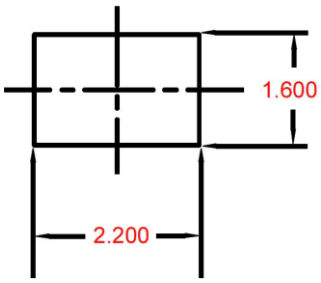
5\ Termination specifications

5.1\ Power terminations, Pads 11, 12, 14 and 15



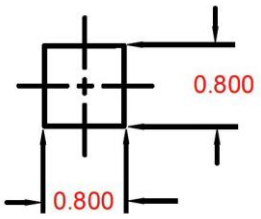
Recommended PAD Size (in mm)

5.2\ Large Signal Pad terminations, Pads 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 13, 17, 18



Recommended PAD Size (in mm)

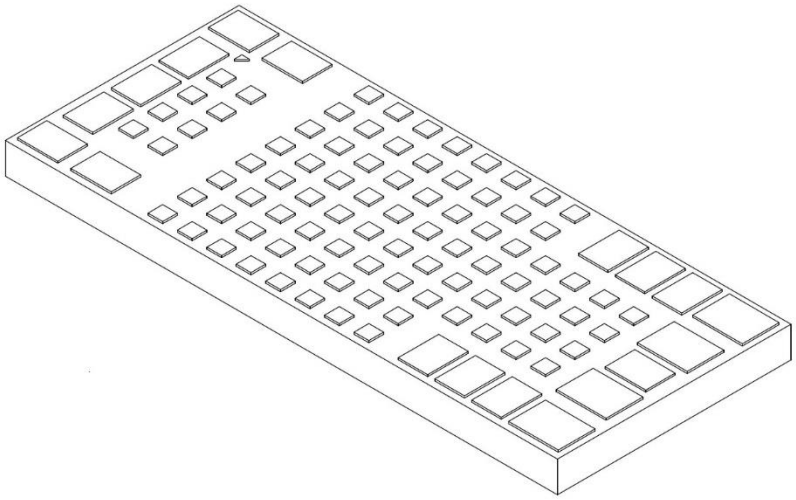
5.3\ All Small Signal Pad terminations



Recommended PAD Size (in mm)

6\ Generic main stamp viewed from the bottom

The main stamp will be terminated with pads that will be soldered on to the pads of the host applications PCB.



7\ Module address setting.

The setting of the address of the module by resistor value is a standard function and is described as;

PSA Stamp addressing		Resistor_down (on the host board)		Resistor_UP (inside the main unit)	
7-Bit based address (SMBus)	8-bit Based address (PMBus)	Resistor series	Resistor value [Ohms]	Resistor series	Resistor value [Ohms]
0x5C	0xB8	E12	OPEN	E12	10,000
0x5A	0xB4	E12	220,000	E12	10,000
0x59	0xB2	E12	120,000	E12	10,000
0x58	0xB0	E12	82,000	E12	10,000
0x74	0xE8	E24	62,000	E12	10,000
0x72	0xE4	E96	48,700	E12	10,000
0x71	0xE2	E12	39,000	E12	10,000
0x70	0xE0	E12	33,000	E12	10,000
0x6C	0xD8	E48	27,400	E12	10,000
0x6A	0xD4	E48	23,700	E12	10,000
0x69	0xD2	E96	20,500	E12	10,000
0x68	0xD0	E48	17,800	E12	10,000
0x64	0xC8	E96	15,800	E12	10,000
0x62	0xC4	E96	13,700	E12	10,000
0x61	0xC2	E48	12,100	E12	10,000
0x60	0xC0	E96	10,700	E12	10,000

8\ Application Block Diagrams

8.1 Isolated block diagrams

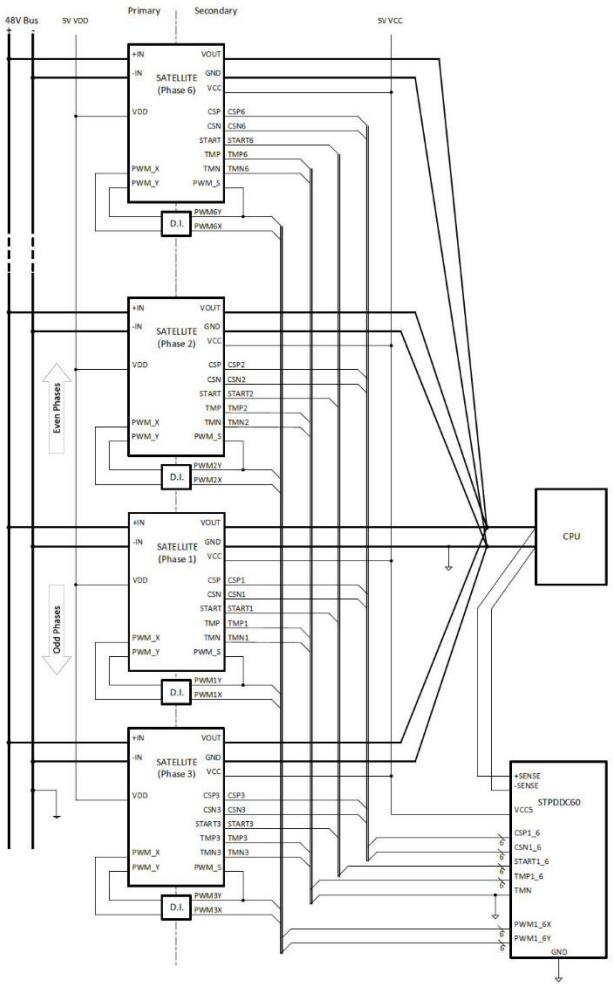
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamps (on the left),

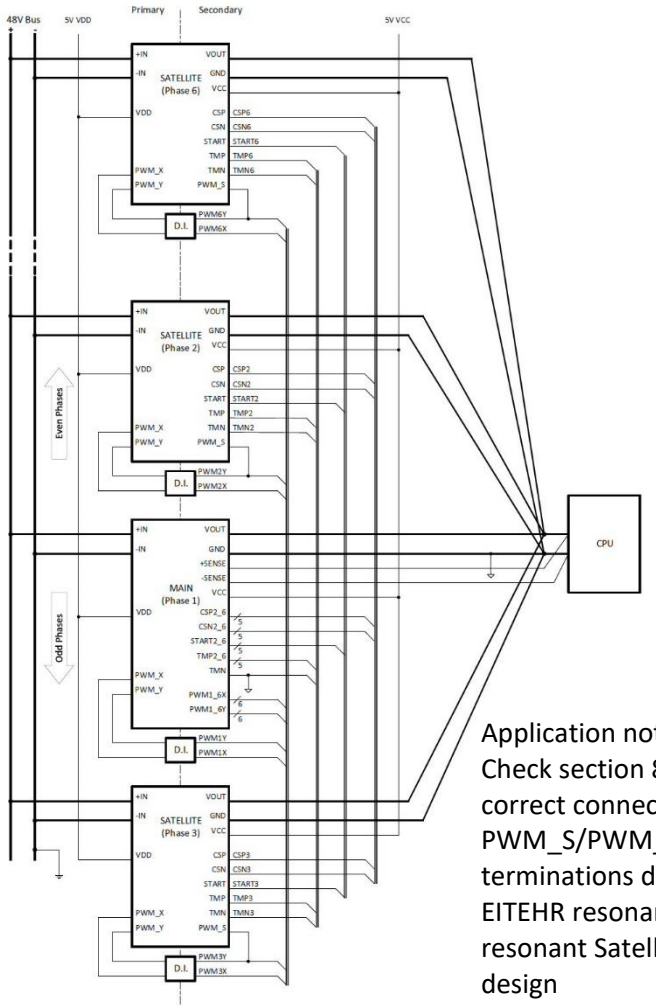
or,

- The Main Stamp plus Satellite Stamp configuration where the main incorporates the controller to control the satellites within itself.

The Power stages are isolated, and the isolation of the signals is provided by the function of the external digital isolator component shown as “D.I.” in the diagrams



Isolated architecture with Controller-IC + Satellites



Isolated architecture with Main+ Satellites

Application note;
Check section 8.3 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

8.2 NON-Isolated block diagrams

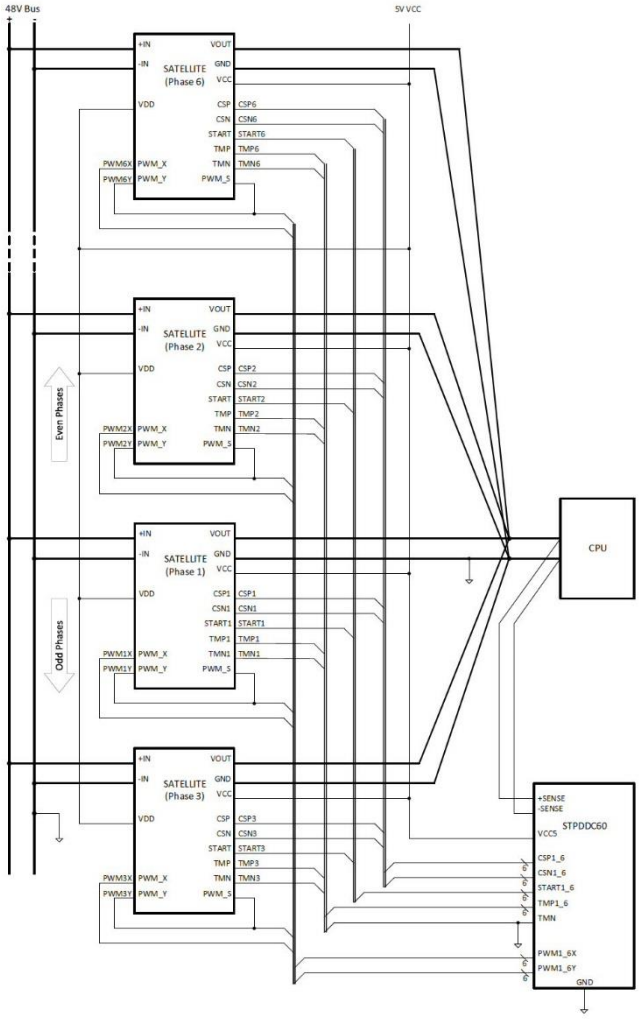
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamps (on the left),

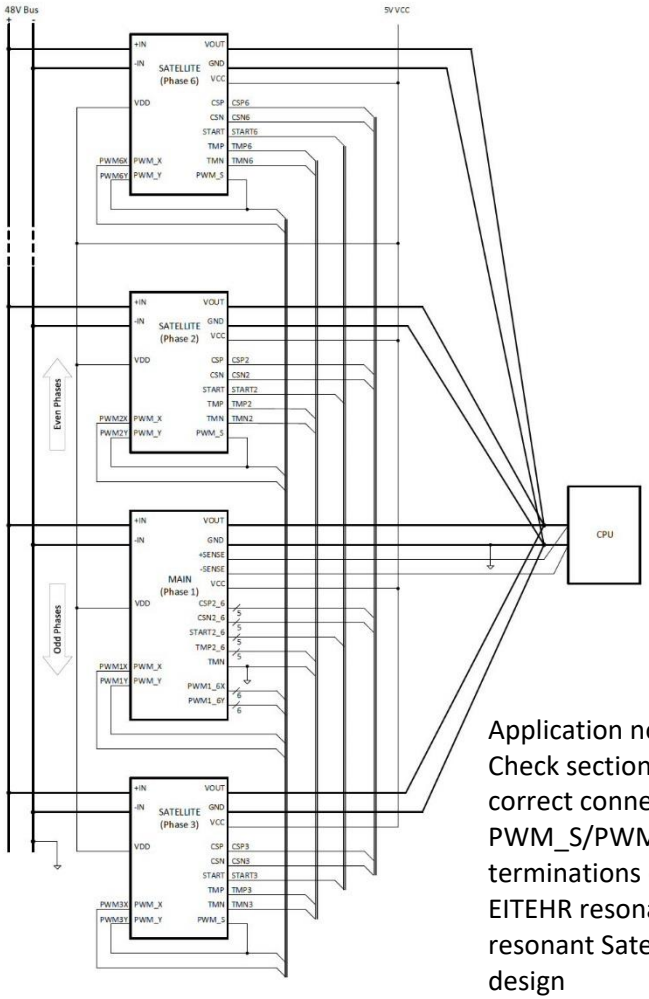
or,

- The Main Stamp plus Satellite Stamp configuration where the Main incorporates the controller to control the salves within itself.

The Power stages are isolated, however, in this configuration the digital isolator component can be eliminated from the network.



Non-Isolated architecture with Controller-IC + Satellites



Non-Isolated architecture with Main+ Satellites

Application note;
Check section 8.3 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

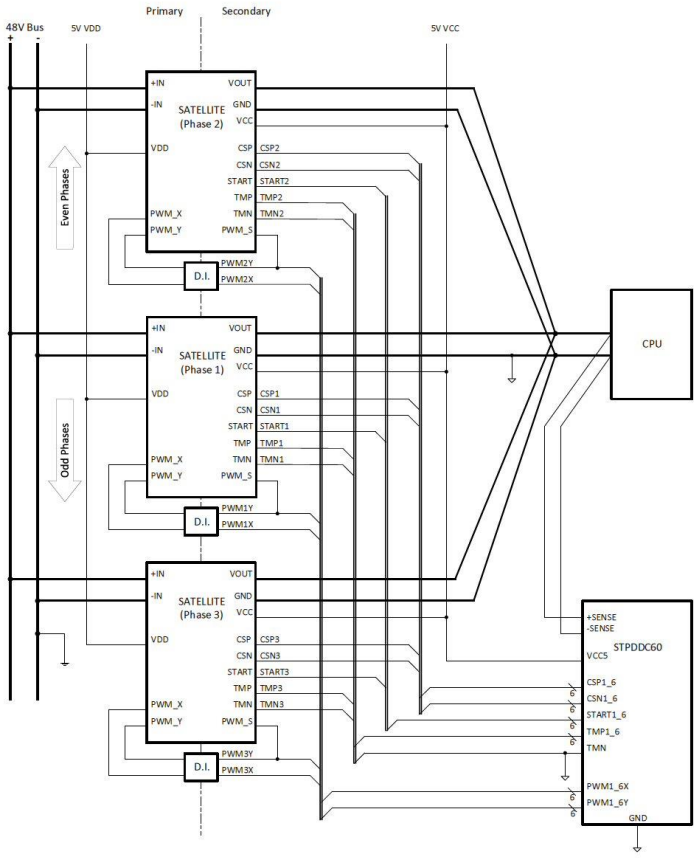
8.3 Relative phase locations

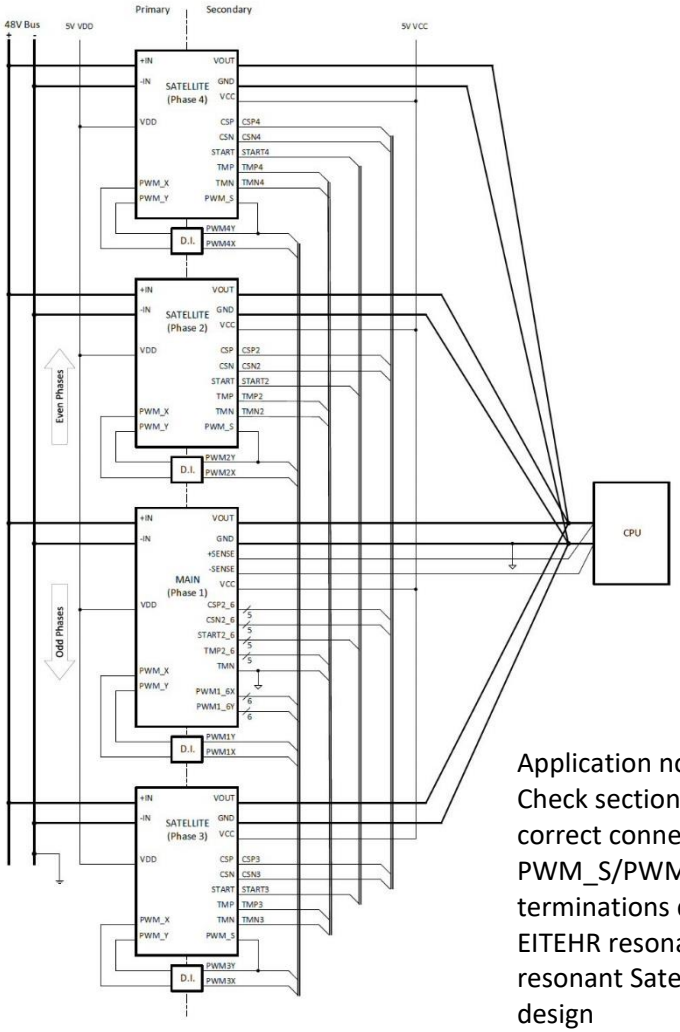
The diagrams show where the PSA recommend the sequential placement of the individual phases in relative terms to each other and the target load device. The rules are;

- To start from the centre
- To group odd and even phases

These 2 rules are recommended if phase-shedding is to be employed, and best possible control response of the network of converters can be achieved

The diagrams show examples of isolated networks of units with both an external controller, or Main Stamp plus Satellite Stamp configuration.





Application note;
Check section 8.3 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

8.4\ Consideration of Non-Resonant and Resonant Satellite stamps

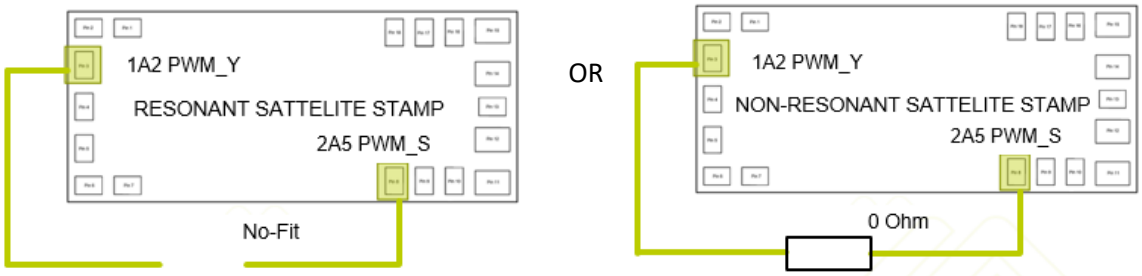
When both types of PowerStamp design approaches are to be accommodated in the same application, there is one consideration to make which is the connection of pin 2A5.

To accommodate both Resonant and Non-Resonant stamps in the same application the following action is needed in application tracking

2A5 to **EITHER** be A floating connection to accommodate Resonant Stamps **OR** A connection to PWM_Y

Accomplish this by applying a Fit or No-fit Zero-Ohm links that is

- Fitted if a Non-resonant stamp is used
- Not fitted if a Resonant stamp is used.



8.5\ Application Safety Standard compliance.

All applications require an appropriately selected protection element incorporated into the input path to each group or interconnected network of Power Stamps with single output voltage. I.e. each Power Stamp group or network must have a correctly selected fuse on its respective input.

The Power Stamp footprint complies to creepage and clearance distances as defined for functional insulation between V-in and 0V respectively and allows for functional or basic insulation between primary and secondary sides. Applications and designs where Power Stamps are used would be compliant to safety standards when the application has been tested to withstand electric strength tests for functional insulation as defined in the standards IEC60950 and IEC62368 respectively. I.e. when tested with a short-circuit applied within the application to simulate a single fault condition.

9\ Standard functions

9.1\ Voltage control

The PSA Main Stamp is a multi-Satellite controller with a complete control logic and protections to realize a high-performance high-efficiency step-down DC-DC voltage regulator optimized for advanced microprocessor, memories and ASIC power supply with direct conversion from 48V bus.

The control loop is based over the high performances Digital STVCOT™ which allows to have fast load transient response neglecting beating effect while maintaining a nearly constant switching frequency in steady state allowing to minimize the output filter components.

The Main Stamp reads the current information delivered from Satellite Stamps. With this information, the Main adjusts the control signal sent to the Satellites in order to equalize the average current carried by each Cell.

In order to guarantee the load to be safe under all circumstances, a complete set of protection is available on output voltage/current, input voltage/current, feedback disconnection, temperature, input/output powers and catastrophic fails.

Energy proportionality features modify the number of active Satellites to optimize the efficiency over the whole load range.

All the required parameters of both the control loop and power management features are programmable through dedicated PMBus™ commands

9.2\ Load shedding and Energy proportionality,

The PSA Main Stamp is capable to support CPU-Link bus-driven power state command to improve the overall conversion efficiency by shedding Satellites and entering Pulse-Skip mode. Through the PMBus™ reconfigurability, these features can be enabled regardless of the command issued through the CPU bus (either SVI or AVS), allowing the optimization of the conversion efficiency in every instant of the conversion.

Satellite Shedding allows the number of working cells to be adjusted according to the delivered current still maintaining the benefits of the multi-cell regulation. The end user can program switch-over threshold in [A] for every cell number transition, with hysteresis. Sleeping Satellites are reset in case of dynamic voltage transitions

9.3\ Output Voltage Positioning

Output voltage positioning is performed by programming properly the digital control loop parameters and (optional) droop function effect using the dedicated PMBus™commands. The Main Stamp Unit embeds a remote-sense buffer to sense remotely the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated compensating for board and connection losses. Keeping the sense traces parallel and guarded by a power plane results in the common mode coupling for any picked-up noise.

The controller reads the current delivered by the additional Satellite units through the CSPx/CSNx pins generating an internal error, which is added to the remote buffer output causing the output voltage to vary accordingly thus implementing the desired load-line effect.

The output voltage setpoint can be configured to be programmed through PMBus™ (supporting standard commands such as VOUT_COMMAND, MARGIN, VOUT_MODE, etc..) or the high speed dedicated CPU link that can be further configured as SVI or AVS. The support of AVS or SVI is mutually exclusive and must be configured prior the unit to be turned enabled for regulation.

9.3.1 SVID control functions.

The PSA Main Stamp is fully compliant with the Intel® VR13 PWM rev 1.6, document #544905 and the Intel® SVID protocol Rev1., document # 456098 within the limitations of VR13.HC. To guarantee proper interactions between VR and CPU, refer to these documents for bus design and layout guidelines. Different platforms may require different pull-up impedance on the CPUI-Link bus. Impedance matching and spacing must be followed. Refer to the PSA member own documentation for the list of supported features.

9.3.2 AVS Support

The PSA Main Stamp is compliant with PMBus™ specification rev 1.3.1; 13 March 2015 – Part III related to the AVSBus support. Refer to this document for bus design and layout guidelines. Refer to the PSA member own documentation for the list of supported features.

The Main Stamp Unit features a digital control technique: a fast analog-to-digital converter (ADC) digitizes the error in the regulation. The resultant digital error signal is then fed into a digital PID compensator and then processed by the Digital STVCOT™ control logic generating the logic signals to drive the Satellite Stamps.

In the case of high-performance digital load, it may be the case the control loop has to be designed for a controlled Output Impedance behaviour, typically in the range of the droop function load line programmed statically (DC). The bandwidth of the system has then to be designed in order to maintain the droop effect programmed in DC even over frequency, taking also in account the output capacitor bank mix and the board parasitic effects.

9.4\ PMBus command set

The PSA Main Stamp is fully compliant with the PMBus™ specification part I and part II, revision 1.2 and with Part III, Revision 1.3.1 (www.pmbus.org). Main Stamps are fully compatible with the PMBus™ specification for read/write access in the byte, word and block mode.

Refer to your PSA member own documentation for the full set of supported PMBus™ commands and features.

9.5\ Telemetry and Protections

The Main Stamp Unit monitors input/output voltages, powers and current in order to manage OV, UV and OC events and to provide telemetry data to the CPU-link and PMBus™ interfaces. According to standard PMBus™ implementation, each protection features a programmable warning and fault limits and actions. Protections can additionally be configured to trigger special outputs such as FAULT pin and SM_ALERT# assertion.

Some of the variables monitored are directly monitored through dedicated ADC while others are computed starting from the available data. Any variable that is computed uses consistent data, i.e. data that refers to the same averaging period.

Refer to your PSA member own documentation for further details of telemetry and protection setting, accuracy and programmability

9.5.1 Black Box Recorder

The black box feature is aimed to picture precisely the status of the device at the fault occurrence. The device records the status of the configured flags before (OLD) and after (NEW) a fault event occurred and stores it into dedicated NVM sectors. The BBR picture is recorded into the device NVM and the information is preserved even in case of power cycling and/or re-trigger of the same protection. The dedicated reset command has to be issued to clear the BBR content.

9.6 Enable function (En, pad L6)

The Enable (En) function of the control stamp will be defined as “positive enable” or “Active high” defined as;

- input high, rising >0.7Vdc
- input low falling <0.4Vdc

The EN pin is un-biased so it needs to be either pulled high or low – it cannot be left floating. The functionality of EN pin differs from VCCIO_OK (L7) that is aimed to sense VCCIO line in VR13HC application to implement a fast protection in case the VCCIO bias goes missing. VCCIO_OK must be shorted to VCC in case it is not used.

10\ Change History

This document is subject to change at any time pending the agreement of the founding membership of the PowerStamp Alliance.

Issue	Date	Issued by	Change
1		A.Brown	- First revision
1.1	20th Oct 2017	A.Brown	- Add the envelope descriptions - Add functional descriptions. - Add the annotated drawing for the signal connections - Add generic power-stamp footprint figure.
1.2	23rd Oct 2017	A.Brown	- Revise and accurately describe the Pad dimensions. - Updated footprint drawing added
1.3	28th Oct 2017	A.Brown	- Update of function table. - Add the Module address setting resistor values.
1.4	21st Nov 2017	A.Brown	- Update of footprint to give 0.5mm space around the primary and secondary pads to the edge of the PCB - Update of Pad 5 name from VSS to VDD - Added application block diagrams – section 7.
1.5	22nd Nov 2017	A.Brown	- Update to the input voltage - Update made to the AVS and SVID control description - VCC description added - VREG description added - -in signal pad description added - Added Host PCB footprint information – section 6
1.6	29th Nov 2017	A.Brown	- Updated pad numbering convention - Updated mechanical drawing information - Updated application block-diagrams with external supply bias shown
1.7	5th Dec 2017	A.Brown	- Update of signal pad table and naming convention. - M5 = Vreg - M6 = VCTRL – Controller supply voltage. - PMBus pads re-named G7, G8, H7, H8 - SVID pads re-named to include mutually exclusive function. - E8, F8, remote sense functions shown as +S, -S - The block diag's updated to show PWM_X position.
1.8	5th Dec 2017	A.Brown	- Updated pad 1A3 name from VSS to VDD
1.9	11th Dec 2017	A.Brown	- Update to drawing – section 2.1 – colour updated and pad-1 reference updated. - Pad A5 and B5 description in 3.2 updated. - Pads J7, J8 and K8 updated to show AVS function. - "Pin" replaced with "Pad"

Issue	Date	Issued by	Change
1.10	14th Feb 2018	A.Brown	Standardized control functions added to the spec. Changed 'Master' to 'Main' Changed 'Slave' to 'satellite'
1.11	16th Feb 2018	A.Brown	Update of interconnect drawings reflects new names
1.12	07 March 2018	R.Vai	Updated section 8
1.13	22nd May 2018	A.Brown/R.Vai	- Added section 1.1 for safety standard compliance and fusing requirement - Updated mechanical drawings - Updated signal names for G7 and L8 - Changed section 6 to show the generic termination of the Main Stamp. - corrected section 7.1 and 7.2 to be in line with 'Main' and 'Satellite' terminology - Added IPC9592-B note to section 3.3 - Added detail 'A' and 'B' to page 8 - Added section 8 – common control function. - Updated outline footprint notes section 3.3
1.14	29th June 2018	A.Brown	- Relocation of safety compliance information. - re-numbered sections
1.15	17th July 2018	A.Brown	- Added legal statement at the end of the document
1.16	June 2020	R. Vai	- Updated notes to Table of Signal pads and descriptions - Updated Module address setting Table specifying 7bit based address - Added section 9.6
1.18a	01st February 2022	R.Vai / A.Brown	- Updated tolerances from +/-0.25mm to +0.4/-0.1mm - Updated pin functional descriptions. - Added notes to each block diagram to refer to section 8.3 on connection of satellites. - Added Section 8.3 to detail the correct connection of pins 2A5 and 1A2 - Updated pins description

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