Increasing Current Capability in PSA-Satellites Applications

Background

Artificial intelligence, machine and deep learning are the latest developments in computer science and allow the generation of a lot of data to optimize the end user experience when browsing the internet and the most-used social media. This is driving the industry to develop powerful ASICs and equipment that currently has a roadmap of up to 1000A in current consumption.

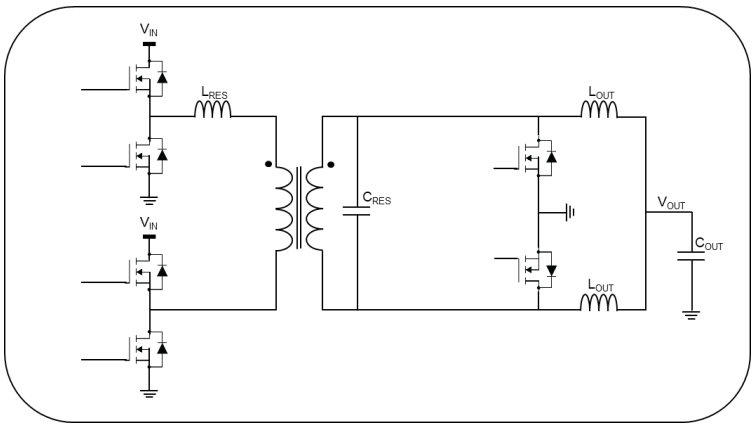
This paper describes how to parallel satellite stamps in order to increase the total current capability of the application. The paper takes into consideration all the effects that may affect current sharing between paralleled stamps and composing them statistically to get the total accuracy.

The Columbus Topology

Power Stamp Alliance (PSA) satellites stamps are built based on the Columbus Topology patented by STMicroelectronics. When approaching the power delivery for a digital load with high load current and fast dynamic response requirements, the traditional isolated topologies generally fail. When approaching the dynamic loading response required, and when considering the scalability and the support of high frequency load-transients, the Columbus architecture naturally manages these challenges. Since the resonant network is excited only during the Ton generation, the resulting design equations are easy and comparable with the traditional multiphase-buck. The control loop based on the STVCoT™ algorithm naturally manages the high-frequency load transients, avoiding the undesirable beating effect. Scalability and light load management are fulfilled thanks to the multi-stamp approach and by the support for PFM native in CoT architectures.

The architecture can be be configured as a resonant or non-resonant converter in order to optimize the design for current capability vs. transient requirements.

From the picture on the right it is possible to observe how the stamp can be configured as resonant or non-resonant simply removing few components. The paper now considers the current sharing resulting when paralleling two stamps being driven by the same PWMX, PWMY and START signals.



Concept Diagram of a Stamp

The critical parameters for each of the topologies are highlighted and changed considering typical production spreads. The current sharing is then analysed by using a Simplis model depicting the topology under analysis. Results are collected and composed considering RSS methodology.

Resonant Configuration

When configured as resonant, each of the stamps shows a native output resistance Req, given by the resonant network. This resistance helps in reducing the current imbalance caused by asymmetries as the load increases. The output impedance can be computed as:

$$Req = Fsw \cdot \alpha \cdot \frac{Lout \cdot Lres}{2 \cdot (Lres + N^2 \cdot Lout)} [1]$$

As the stamp features an intrinsic output resistance, the current sharing error is mitigated as the load increases, resulting in a recirculating current at zero load that progressively disappears as the load increases.

The two dominant parameters in causing an imbalance effect on the output are:

- The resonant network (Lres and Cres)
- The output inductor (Lout).

The effect of any other parameter is negligible.

Typical tolerances are in the range of 20% (5-sigma distribution). Since the components mentioned above refer to different and independently-manufactured components, the variables can be considered as statistically independent. The simulation of the single-contributor can then be composed with the RSS method so still obtaining a 3-sigma imbalance current effect. The linear sum of the components will result in a 9-sigma worst-case analysis (though unrealistic).

Variable		Max Tolerance	Effect on Current Balance	
			No Load [+/-A]	Full Load [+/-A]
A	Resonant Inductor (Lres)	+/-10%	14.5	1
B	Resonant Capacitor (Cres)	+/-10%	12	3
C	Output Inductor (Lout)	+/-10%	7.5	2
3-sigma composition				
RSS		Sqrt(A^2+B^2+C^2)	20	3.7

Non-Resonant Configuration

When configured as non-resonant, each of the stamps does not show any native output resistance: the resonant network is not present, and the application cannot benefit from it.

The dominant parameters in causing an imbalance effect on the output are:

- The driver PWM processing skew
- The parasitic resistance (DCR) of the output inductors
- The transformer leakage inductance and output inductance tolerances
- The synchronous rectifier mosfets RdsOn

As per the previous (resonant) case, all the above variables are to be considered as statistically independent and can be composed using the RSS methodology. In this case, the imbalance is basically load-independent, unless considering a second-order effect of how any of the parameter may differently change as the current increases (i.e. an inductance saturation effect). The linear sum of the components will result in a 9-sigma worst-case analysis (15A; though unrealistic).

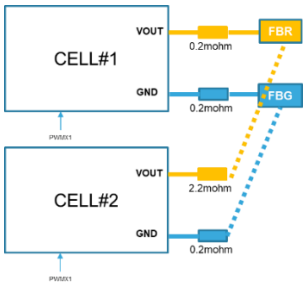
	Variable	Max Tolerance	Effect on Current Balance [+/- A]
A	PWM Skew	+/-10nSec	10
B	Output Inductor DCR	+/-10%	0.5
C	Leakage Inductance (Trasfo)	+/-10%	2
D	Output Inductance (Lout)	+/-10%	1
E	Synchronous Rectifier Mosfets RdsON	+/-10%	1
3-sigma composition			
RSS		Sqrt(A^2+B^2+C^2+D^2+E^2)	10.3

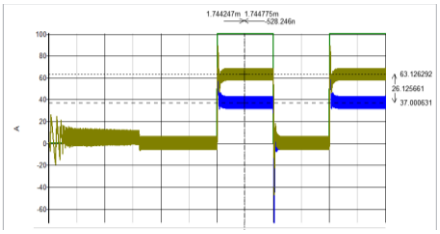
Layout Guidelines: Symmetry

In order to get the best performance in terms of current balance, controlling the symmetry of the layout is mandatory. Any difference in the layout may result in degraded performance of the stamps being connected in parallel. The case being simulated considers closing the loop close to one of the two stamps, so in a non-symmetrical manner. This case also assumes having 0.2mR stray resistance in series to each VOUT/GND connection, the resulting imbalance is then measured.

The imbalance is negligible at no load, but it increases up to +/-13A at 100A (full-load).

It is recommended to maintain the maximum symmetry in the layout placement of the paralleled stamps. In particular, it is mandatory to maintain the two stamps as close as possible to avoid the creation of parasitic that will compromise the symmetry.





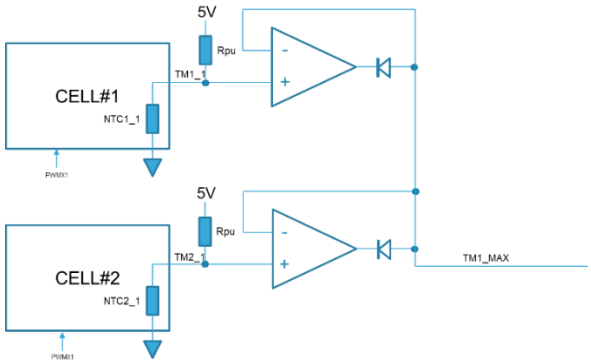
200A load transient over two paralleled stamps with non-symmetric feedback connections

Temperature sense

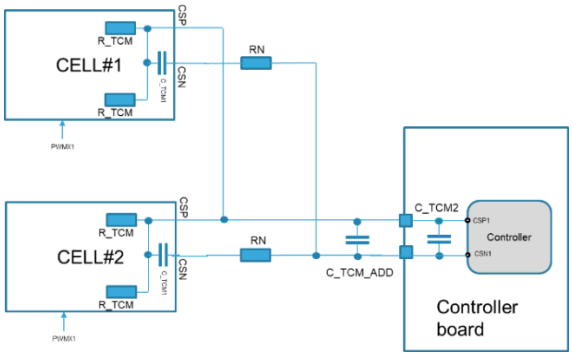
Different approaches may be considered when connecting the temperature feedback of two stamps.

The first, and easiest, approach consists in simply parallelizing the two connections. This will result in the sense from the controller stamp of the average temperature between the two satellite stamps.

Alternatively, by using the circuit depicted below, it is possible to isolate the maximum between the two temperature in order to maintain control on the hot spot of the application.
The circuit below must be adopted for each of the pair of stamps connected in parallel and it reports the max temperature between the pair.



Temperature Sense Connections



Current Sense Connections

Current Sense Connections

The last item to be considered when paralleling stamps is the current reporting: it is suggested to add a small 10R resistor in series to the CSN pin of the pair of satellite stamps in order to compensate for the slight differences there might be between the CSN connection of the adjacent stamps. Even if the layout is maintained symmetrically, it may be a good practice to take these differences into consideration in the routing of the PCB.

Conclusion

This paper has analysed the possibility to parallelize stamps in order to increase the solution current capability. By creating symmetrical pairs of power stamps, up to 6 pairs can be successfully realized increasing the total current capability to more than 1000A.

Change History

This document is subject to change at any time pending the agreement of the founding membership of the Power Stamp Alliance.

Issue	Date	Issued by	Change
1		R. Vai	- First revision

References

[1] Stefano Saggini, Osvaldo Zambetti, Roberto Rizzolatti, Massimiliano Picca, Paolo Mattavelli, “An Isolated Quasi-Resonant Multi-Phase Single-Stage Topology for 48 V VRM Applications”, in IEEE Transactions on Power Electronics, vol. 33, no. 7, July 2018, pp.6224 - 6237