Power Stamp Satellite Stamp Unit Specification

1\ Function and feature specification

This description defines the footprint and function of the standard PSA "SATELLITE STAMP" power converter that is to be used in conjunction with the PSA "MAIN STAMP" power converter.

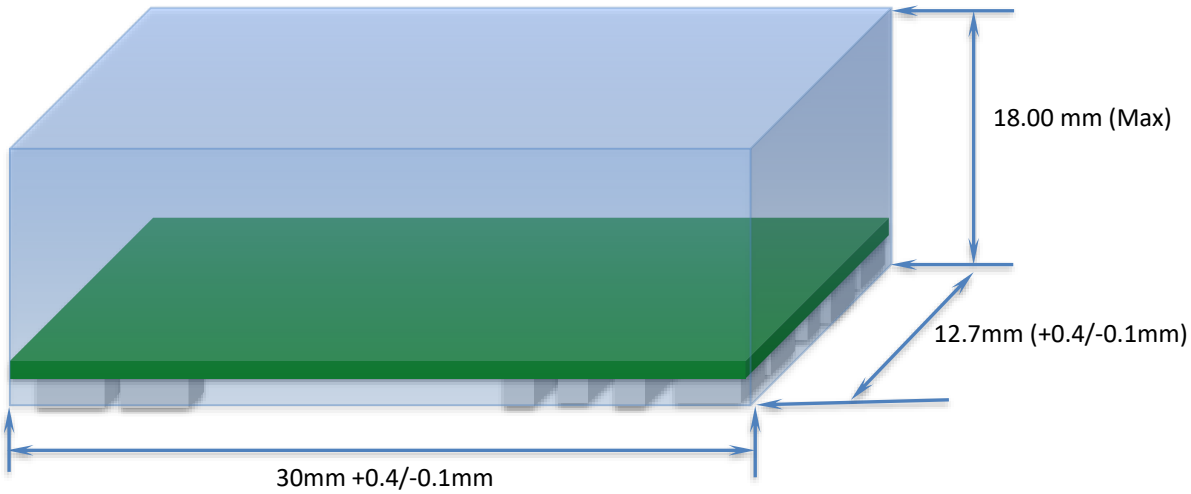
The function of this power converter is to extend the power and current rating of the standard PSA family of products.

Parameter	Specification	Notes
Input voltage	54V nominal 40Vdc to 60Vdc	Input to be <ELV limit
Output voltage	0.5v to 2v5	
Output current	Up to 100A	Expansion stamp current rating

2\ Mechanical details

Power Stamps are defined by the maximum outer envelope dimensions. The length and width are defined and are fixed dimensions. The height defined is the maximum height allowable for designs which may not use the maximum available space

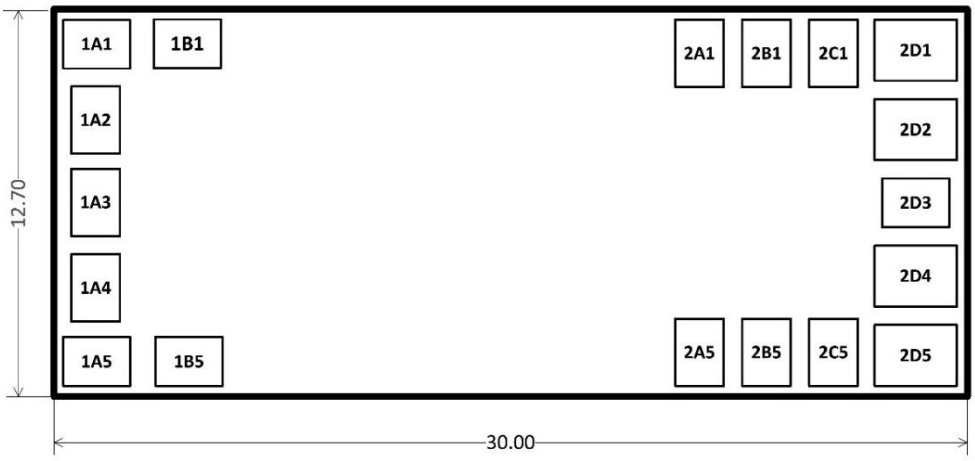
The outer envelope of the power-stamp Satellite Stamp is described as



3\ Interconnect details

3.1\ Pin locations for the PSA Satellite

Bottom view of the module with pin locations and names shown



3.2\ Pin function description for the PSA Satellite Stamp.

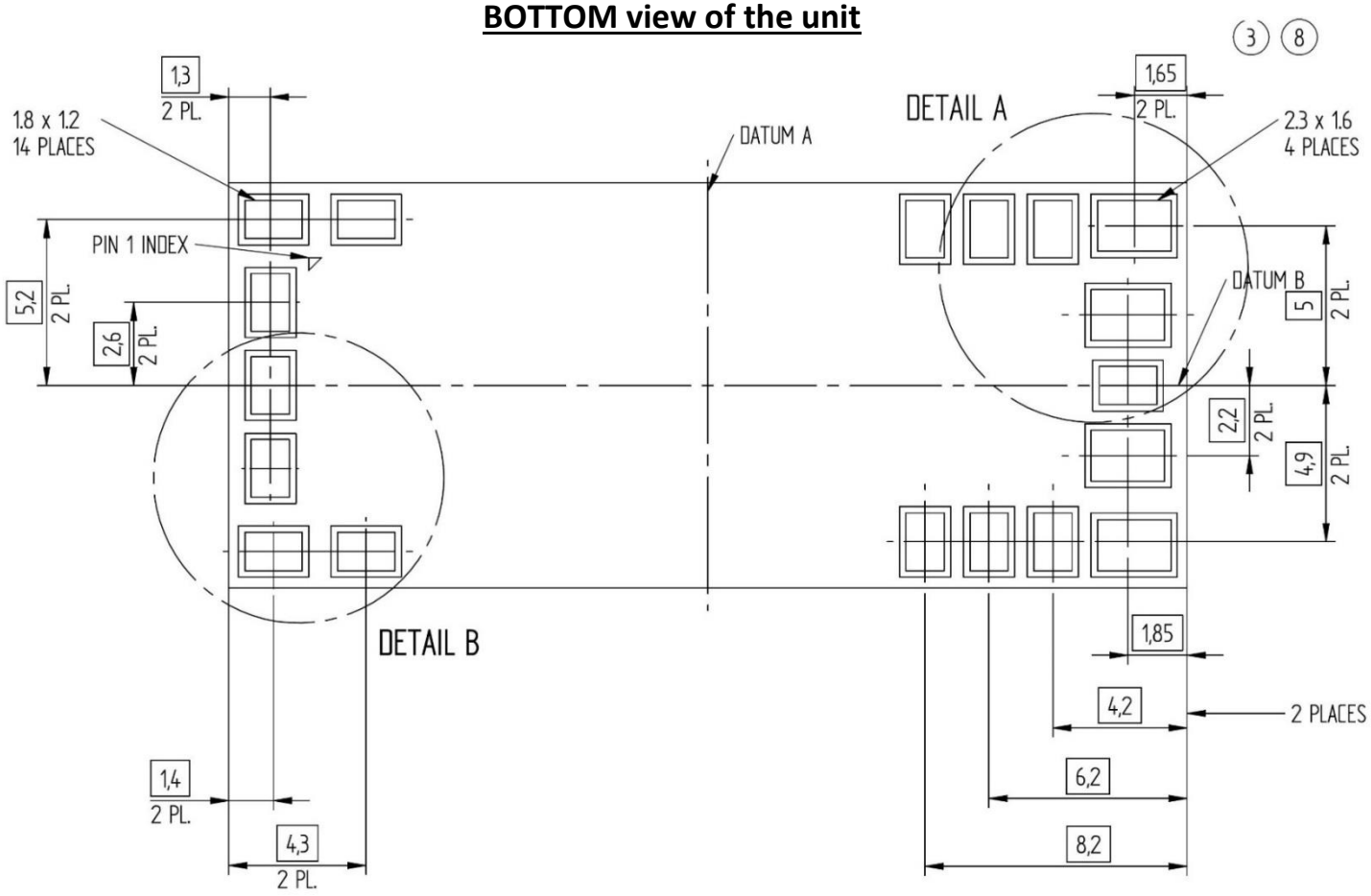
Short descriptions of the individual pins on the unit are;

Pad #	I/O	Pad name	Pad Function
1A1	I	+IN	Positive Input voltage supply connection. Connect with appropriately sized PCB traces for the input power supply and filter locally according to the load performances.
1A2	I	PWM_Y	PWM input Y connection. Connect with the related Controller/Main Unit PWM_Y phase output. Use a digital isolator for the signal in case of isolated topologies.
1A3	I	VDD	Primary Auxiliary voltage supply. Connect external 5V bias or to the controller Stamp VDD pin for correct operation.
1A4	I	PWM_X	PWM input X connection. Connect with the related Controller/Main Unit PWM_X phase output. Use digital isolator for the signal in case of isolated topologies.
1A5	I	+IN	Positive input voltage supply connection. Connect with appropriately sized PCB traces for the input power supply and filter locally according to the load performances.
1B1	n/a	-IN	Primary side ground connection. Connect with PCB primary-side GND power plane.
1B5	n/a	-IN	Primary side ground connection.

Pad #	I/O	Pad name	Pad Function
			Connect with PCB primary-side GND power plane.
2A1	I	START	START signal for secondary driver. Connect with the related Controller/Main Unit START phase output.
2A5	I	PWM_S or N/C	Dual function pin. Refer to section 6.4 for guidance. For Non-resonant Power stamps, connect this pin to the related phase PWM_Y connection. For Resonant Powerstamp, leave this connection as Not Connected.
2B1	O	TMN	Negative Temperature Sense signal output. Connect with related Controller/Main Stamp common temp sense input pin in kelvin connection with TMN (pad 2C1).
2B5	I	VCC	Secondary side Auxiliary voltage supply, connect to external 5V bias or to the controller Stamp VCC pin.
2C1	I	TMP	Positive Temperature Sense signal output. Connect with related Controller/Main Stamp temp sense input pin in kelvin connection with TMN (pad 2B1).
2C5	I	CSP	Positive Current Sense signal output. Connect with Controller/Main Stamp related Current Sense Input pad in kelvion connection with CSN (pad 2D3).
2D1	n/a	GND	Secondary side ground connection. Connect with PCB GND power plane.
2D2	O	VOUT	Positive output voltage connection. Connect with appropriately sized PCB traces to the output load.
2D3	O	CSN	Negative Current Sense signal. Connect with Controller/Main Stamp related Current Sense Input pad in kelvin connection with CSP (pad 2C5).
2D4	O	VOUT	Positive output voltage connection. Connect with appropriately sized PCB traces to the output load.
2D5	n/a	GND	Secondary side ground connection. Connect with PCB GND power plane.

3.3\ The diagram below shows the centre points of the PIN location and PAD size required to host the Satellite Stamp

BOTTOM view of the unit



Notes;

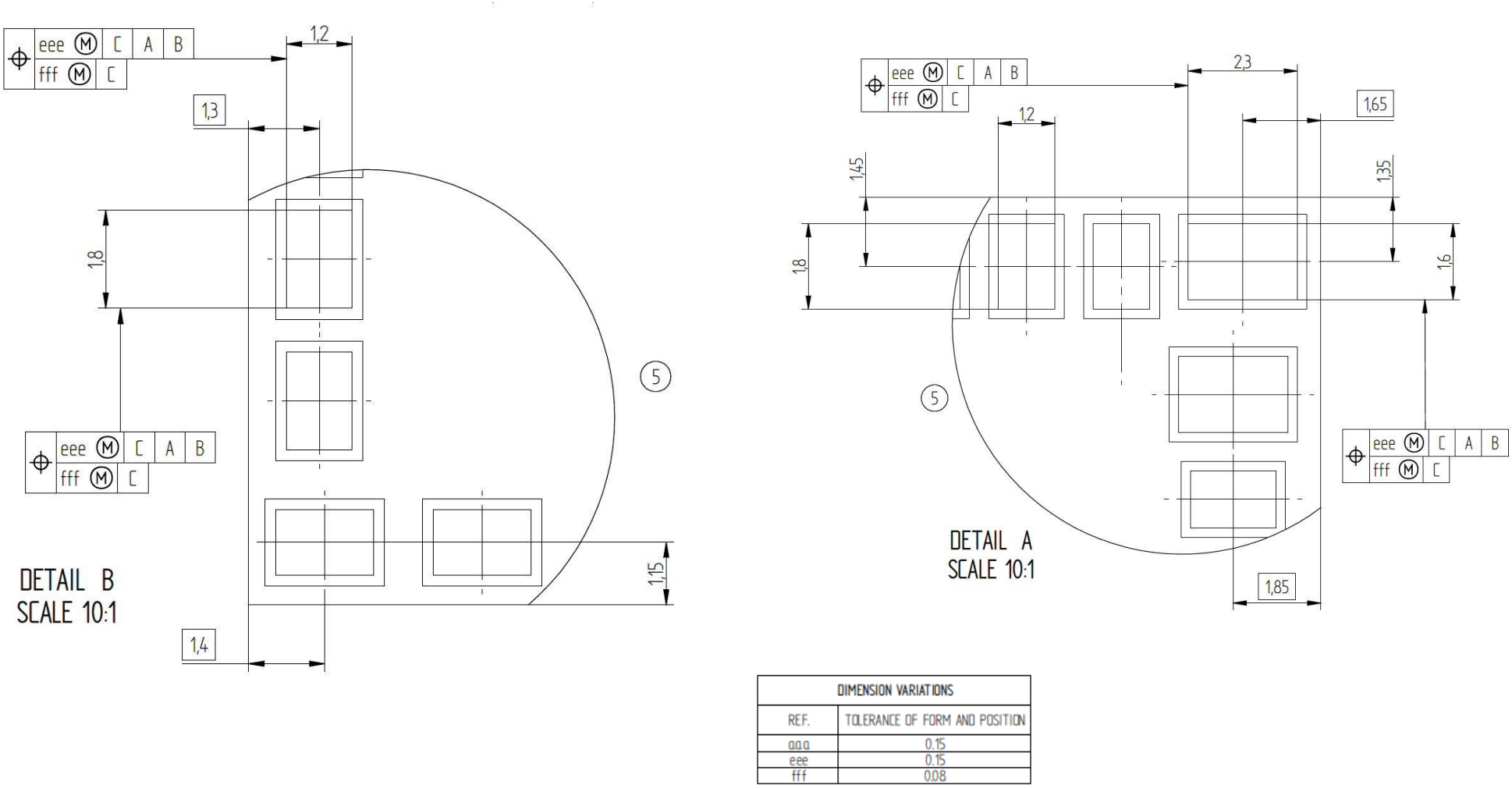
1\ Footprint compliant to IPC7351C and JEDEC JEP95 – DG 4.25, SPP-010, Issue B

2\ Footprint compliant to IPC9592-B guidance;

- Primary positive input to 0V clearance dependant on the implementation of an input fuse and application insulation test
- Primary to secondary; basic insulation provided by footprint. Functional or Basic insulation within the Power Stamp will be dependent on the respective Power Stamp being considered.

2\ Zero Orientation with Pad 1 in Lower Left Corner of the footprint; compliant to IEC 61188-7 and IPC-7351C “Level B”

3.4\ Detail information from the previous figure.



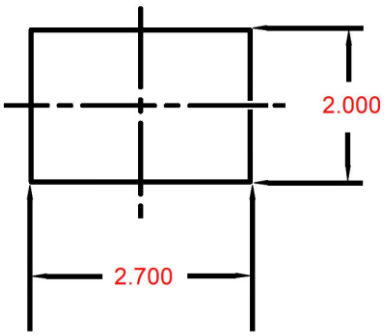
DIMENSION VARIATIONS	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.15
eee	0.15
fff	0.08

4\ Termination specifications

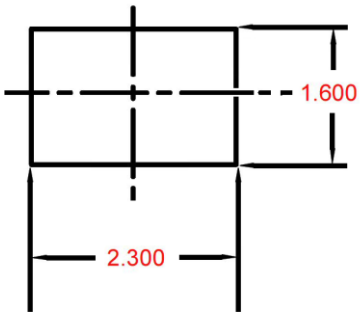
4.1\ Power terminations,

Pins; 2D1, 2D2, 2D4, 2D5

Recommended PAD Size (in mm)



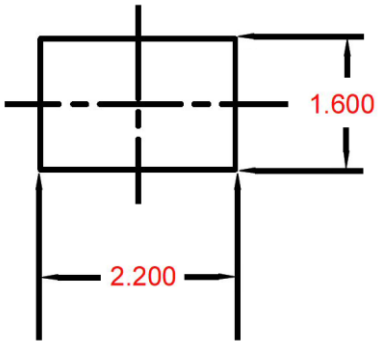
Defined PIN Size (in mm)



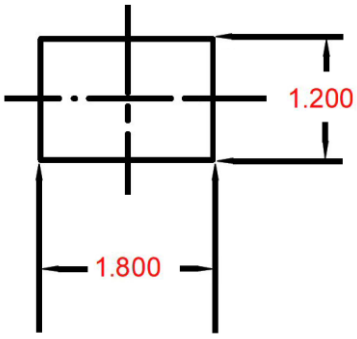
4.2\ Large Signal Pad terminations,

Pins; 1A1, 1A2, 1A3, 1A4, 1A5, 1B1, 1B5, 2A1, 2A5, 2B1, 2B5, 2C1, 2C5, 2D3

Recommended PAD Size (in mm)



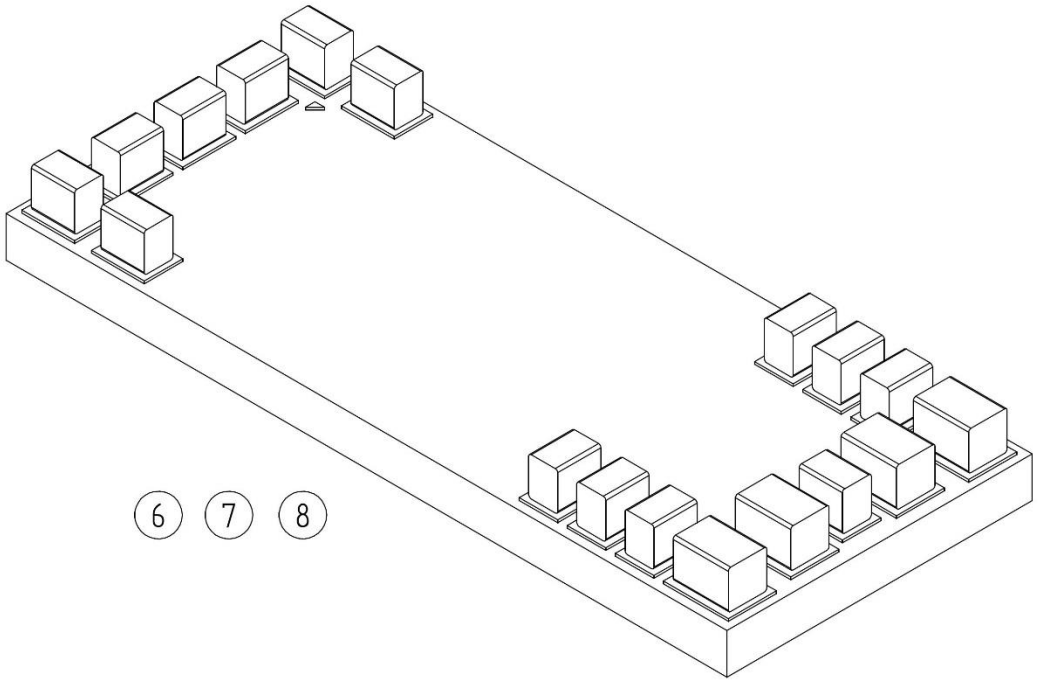
Defined PIN Size (in mm)



5\ Generic Satellite stamp termination

5.1\ Generic satellite stamp viewed from the bottom

The Satellite stamp will be terminated with block pins that will be soldered to the powerstamps PCB, which in turn are to be soldered on to the pads of the host applications PCB.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DATUM "C" IS THE SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED, THE PIN IDENTIFIER MAY BE EITHER A LABEL, A MARKED FEATURE OR A CHAMFERED EDGE
5. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION
6. BOTTOM VIEW OF TYPICAL MODULE PCB SHOWN FOR ILLUSTRATION PURPOSES ONLY
7. OVERALL MODULE HEIGHT NOT TO EXCEED 18mm
8. SEE INDIVIDUAL MODULE DATA SHEET FOR DETAILED TOP AND SIDE VIEW

6\ Application block diagrams

6.1 Isolated block diagrams

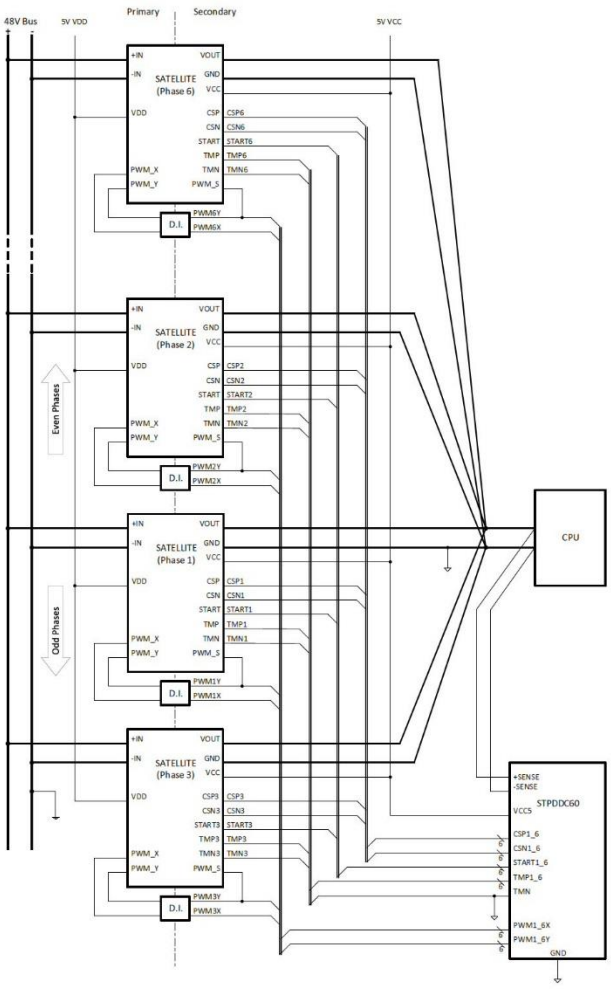
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamps (on the left),

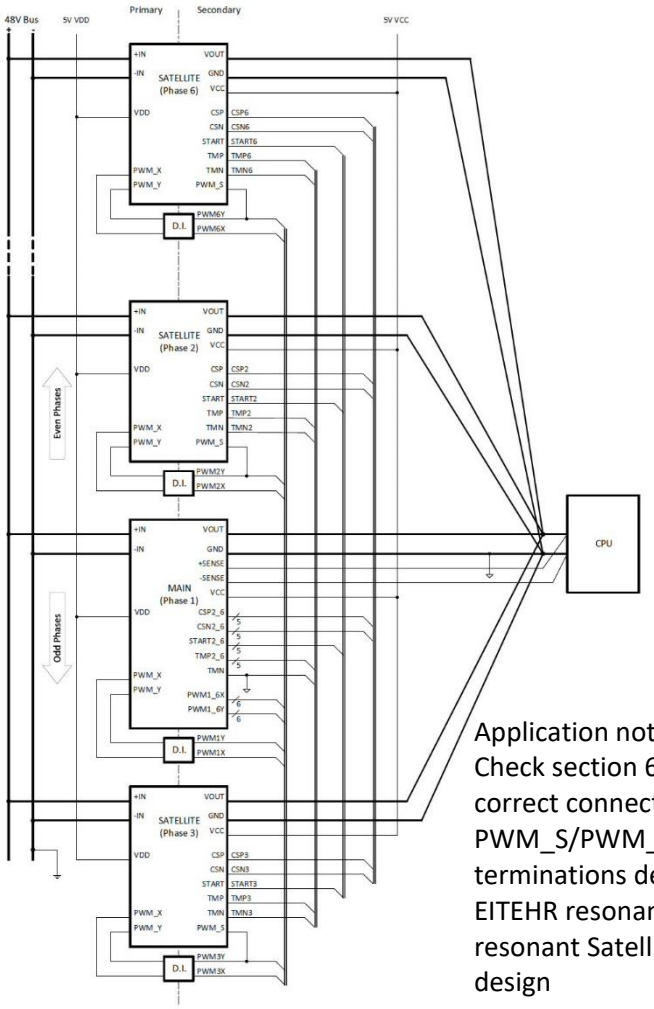
or,

- The Main plus Satellite configuration where the Main incorporates the controller to control the salves within itself.

The Power stages are isolated, and the isolation of the signals is provided by the function of the external digital isolator component shown as “D.I.” in the diagrams



Isolated architecture with Controller-IC + Satellites



Isolated architecture with Main + Satellites

Application note;
Check section 6.4 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

6.2 NON-Isolated block diagrams

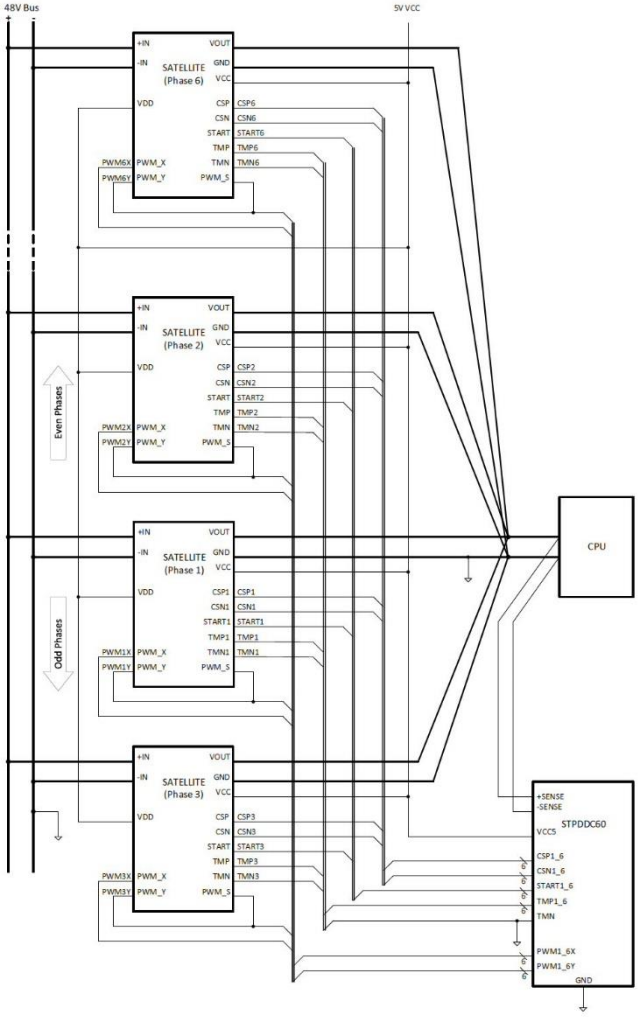
The diagrams show isolated block-diagram connections with either;

- An external controller to control and monitor any Satellite Stamp (on the left),

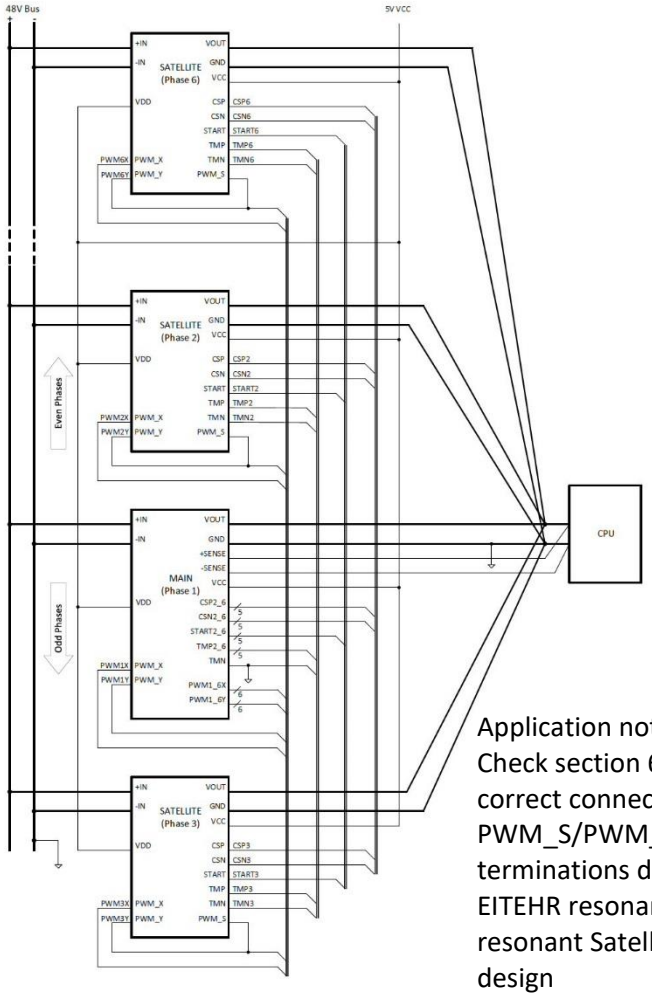
or,

- The Main stamp plus Satellite Stamp configuration where the Main Stamp incorporates the controller to control the salves within itself.

The Power stages are isolated, however, in this configuration the digital isolator component can be eliminated from the network.



Non-Isolated architecture with Controller-IC + Satellites



Non-Isolated architecture with Main + Satellites

Application note;
Check section 6.4 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

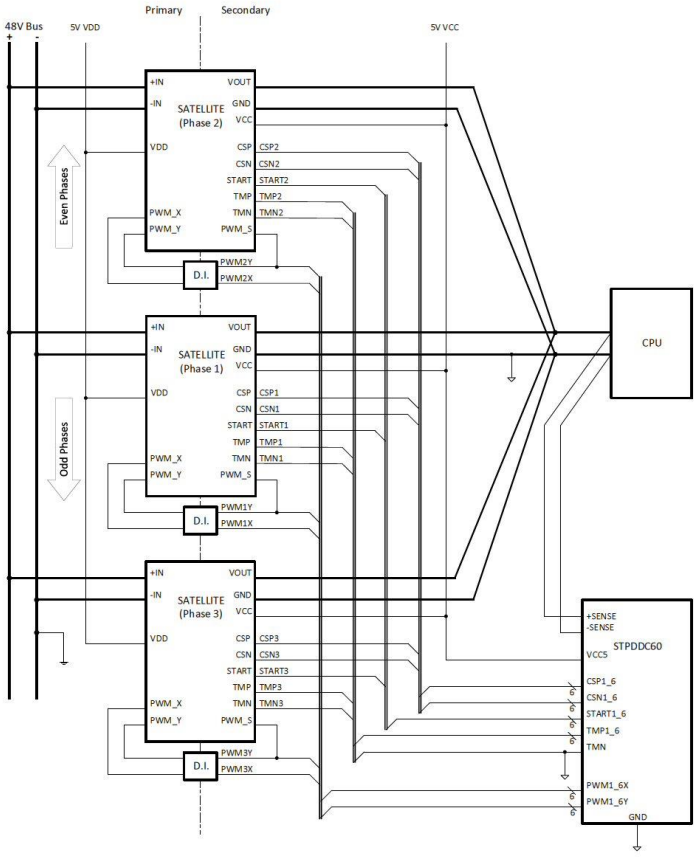
6.3 General note on relative phase-locations to the load

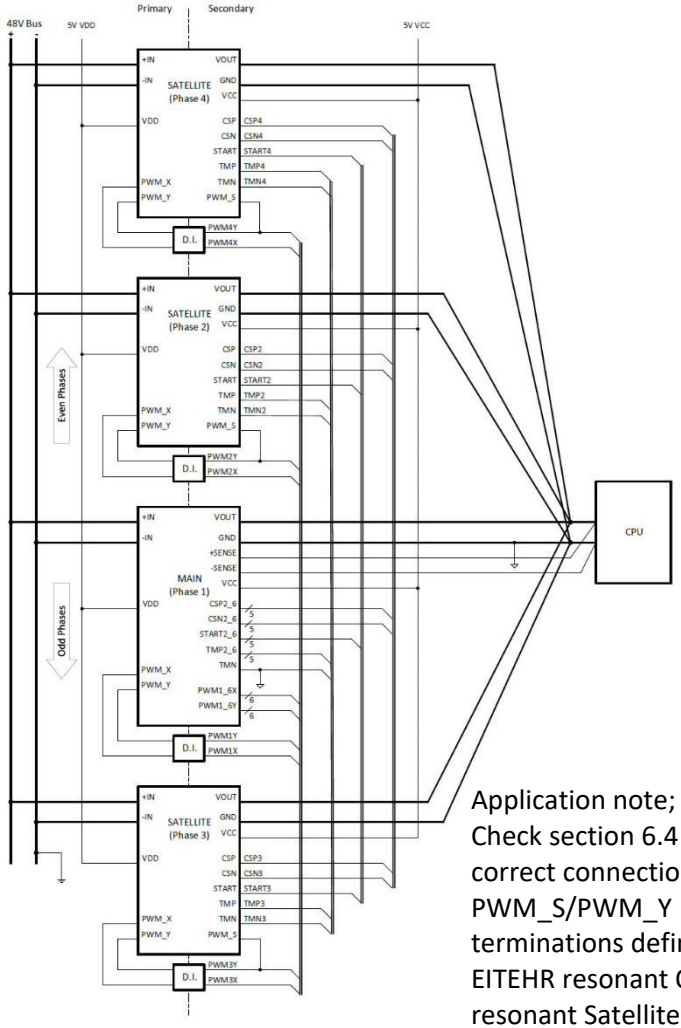
The diagrams show where the PSA recommend the sequential placement of the individual phases in relative terms to each other and the target load device. The rules are;

- To start from the centre
- To group odd and even phases

These 2 rules are recommended if phase-shedding is to be employed, and best possible control response of the network of converters can be achieved

The diagrams show examples of isolated networks of units with both an external controller, or Main Stamp plus Satellite Stamp configuration





Application note;
Check section 6.4 for correct connection of PWM_S/PWM_Y terminations defined by EITEHR resonant OR non-resonant Satellite module design

6.4\ Consideration of Non-Resonant and Resonant Satellite stamps

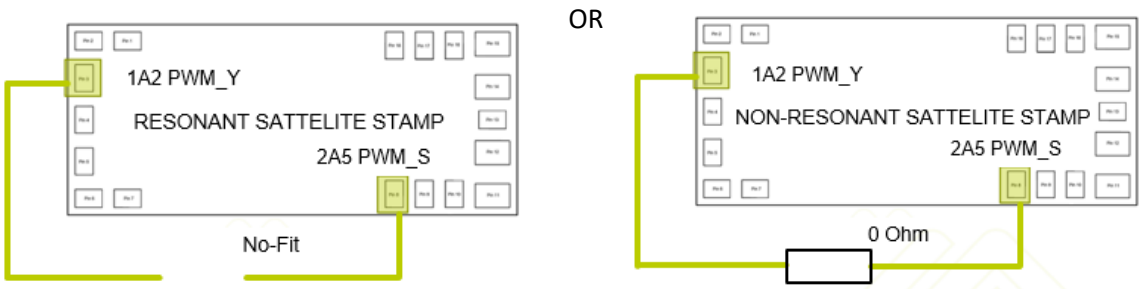
When both types of PowerStamp design approaches are to be accommodated in the same application, there is one consideration to make which is the connection of pin 2A5.

To accommodate both Resonant and Non-Resonant stamps in the same application the following action is needed in application tracking

2A5 to **EITHER** be A floating connection to accommodate Resonant Stamps **OR** A connection to PWM_Y

Accomplish this by applying a Fit or No-fit Zero-Ohm links that is

- Fitted if a Non-resonant stamp is used
- Not fitted if a Resonant stamp is used.



6.5\ Safety compliance.

All applications require an appropriately selected protection element incorporated into the input path to each group or interconnected network of Power Stamps with single output voltage. I.e. each Power Stamp group or network must have a correctly selected fuse on its respective input.

The Power Stamp footprint complies to creepage and clearance distances as defined for functional insulation between V-in and 0V respectively and allows for functional or basic insulation between primary and secondary sides. Applications and designs where Power Stamps are used would be compliant to safety standards when the application has been tested to withstand electric strength tests for functional insulation as defined in the standards IEC60950 and IEC62368 respectively. I.e. when tested with a short-circuit applied within the application to simulate a single fault condition.

7\ Change History,

This document is subject to change at any time pending the agreement of the founding membership of the PowerStamp Alliance.

Issue	Date	Issued by	Change
1		A.Brown	- First revision
1.1	20th Oct 2017	A.Brown	- Add the envelope descriptions - Add functional descriptions.
1.2	23rd Oct 2017	A.Brown	- Revise and accurately describe the Pad and Pin dimensions.
1.3	28th Oct 2017	A.Brown	- Update of function table.
1.4	17th Nov 2017	A.Brown	- Update of footprint to give 0.5mm space around the primary and secondary pins to the edge of the PCB - Update of Pin 5 name from VSS to VDD - Add application block-diagrams
1.5	22nd Nov 2017	A.Brown	- Update of the input voltage specification - Update to section 5 to add the Host PCB footprint information
1.6	29th Nov 2017	A.Brown	- Updated pin numbering convention - Updated mechanical drawing information - Updated application block-diagrams with external supply bias shown
1.7	5th Dec 2017	A.Brown	- Updated the application block diagrams with new net-names shown
1.8	11th Dec 2017	A.Brown	- Updated pin 1A3 name from VSS to VDD
1.9	14th Feb 2018	A.Brown	Standardized control functions added to the spec. Changed 'Master' to 'Main' Changed 'Slave' to 'satellite'
1.10	16th Feb 2018	A.Brown	Update of interconnect drawings reflects new names
1.11	23rd April 2018	A.Brown	- Added section 1.1 for safety standard compliance and fusing requirement - Updated mechanical drawings - Updated signal names for G7 and L8 - Changed section 5 to reflect the 'generic terminations' as opposed to the generic power stamp footprint.
1.12	18th May 2018	A.Brown	- Added IPC9592B comment to section 3.2 - Updated (extended) section 1.1 on safety compliance - Updated figure in 2.1 to be the new footprint.
1.13	29th June 2018	A.Brown	- Relocation of safety compliance information. - re-numbered sections
1.14	17th July 2018	A.Brown	- Added legal statement at the end of the document

Issue	Date	Issued by	Change
1.16	13th January 2022	R.Vai A.Brown	-Updated tolerances from +/-0.25mm to +0.4/-0.1mm -Updated Interconnect descriptions -Section 6.4 added to describe connection of different design approaches - Added notes to each block diagram to reference section 6.4 for resonant/non-resonant stamp connection. -Updated pins description