

Addressing the challenge of increasing the power conversion density in CPU power solutions and evaluation of them,

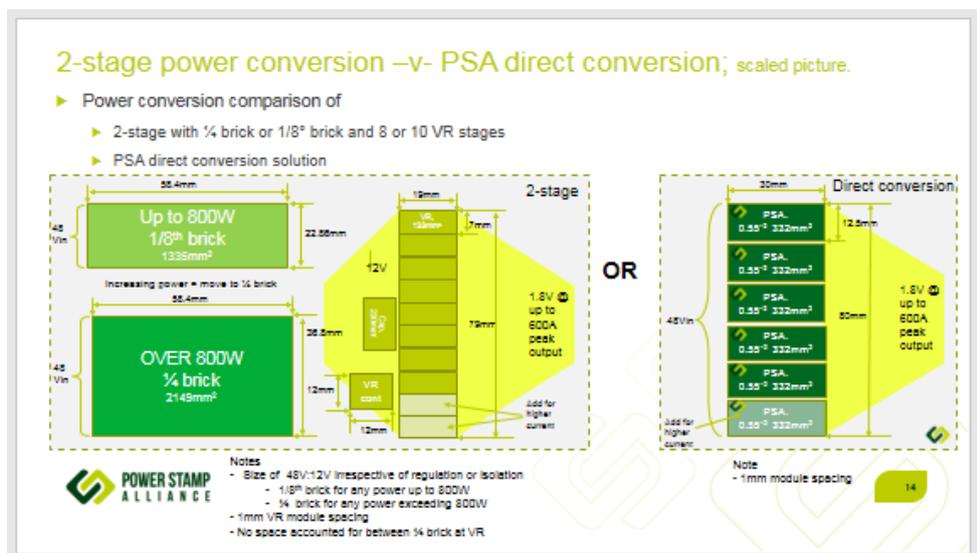
With the steadily increasing power demands of both computing and server applications, several challenges are encountered in realizing power distribution and conversion. The trend toward running systems with a shared 48V distribution voltage at rack or cabinet levels and away from converting from AC to 12V locally within the application does indeed generate significant space within the application, however, the question is how best to deal with the 48Vdc input voltage in the application.

There is just as much pressure (in some cases, more so) on the PCB real-estate usage in the conversion from 48V to the low voltages required by applications. The challenge is how to accomplish this in the smallest size, and, be able to cool the power-conversion stages.

To convert 48V to point of use voltages such as 1V, it is no surprise that the prevalent two-stage architecture, typically made up of an isolated bus converter followed by a non-isolated point-of-load converter, has met its single stage (aka direct conversion) challenger.

The two-stage conversion architecture has its merits, but, one of them is not PCB real estate. The Power Stamp Alliance (PSA) - made up of companies Advanced Energy, Bel Power, Flex, and ST Microelectronics - formed to address the footprint-compatible needs of the direct conversion demand. Achieving a current-density volume of 300 amps/inch³.

Comparing the same power levels when using a 2-stage conversion approach and a direct conversion from 48V to core-power requirements, it can be seen very clearly that up to a 46% saving in PCB-real-estate can be realized by utilizing the direct-conversion design-approach.



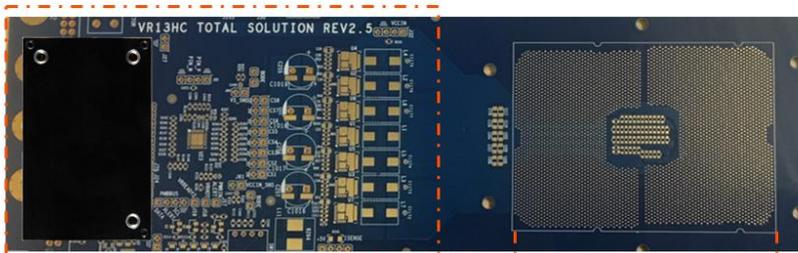
Summary of real-estate reduction by peak power

PEAK POWER	48V:12 stage	Count and size of VR stage	2-stage Total size	PSA stamp Size & density	PCB size reduction & Power density increase
1000W 1v8 @ 300A	1/4 th brick 58.4mm*36.8mm = 2149mm ²	10 VR phase 10 * (19mm * 7mm) = 1501mm ² 1 * VR controller = 144mm ² 12V Capacitors = 200mm ²	3994mm ² 25W/cm ²	6 Power stamps 6*(30mm*12.7mm) total = 2400mm ² 41 W/cm ²	1554mm ² reduction 40% smaller 25 W/cm ² → 41 W/cm ²
800W	1/4 th brick 58.4mm*36.8mm = 2149mm ²	8 VR phase 8 * (19mm * 7mm) = 1197mm ² 1 * VR controller = 144mm ² 12V Capacitors = 200mm ²	3690mm ² 21W/cm ²	5 Power stamps 5*(30mm*12.7mm) total = 1955mm ² 40 W/cm ²	1554mm ² reduction 46% smaller 21 W/cm ² → 40 W/cm ²
800W	1/8 th brick 58.4mm*36.8mm = 1335mm ²	8 VR phase 8 * (19mm * 7mm) = 1197mm ² 1 * VR controller = 144mm ² 12V Capacitors = 200mm ²	2876mm ² 28W/cm ²	5 Power stamps 5*(30mm*12.7mm) total = 1955mm ² 40 W/cm ²	881mm ² reduction 30% smaller 28 W/cm ² → 40 W/cm ²



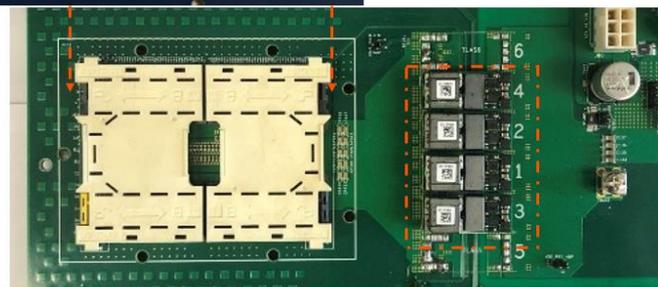
This 40% PCB real-estate reduction for the power-conversion stage that meets the most demanding of applications, however, the challenge always surrounds the dissipated heat from the power converters and how to extract that from the application.

Comparative layouts



- 2-stage conversion
- 1/4 brick shown (Left)
- Feeding power to VR-power conversion stages.
- Input caps to the brick NOT shown here.

- Single stage conversion.
- 4 100A power-stages shown
- 1 Main + 3 satellites.
- All external components shown



- Same CPU socket shows comparative simplification

With LoadSlammer now joining the PSA, the collaboration of power-conversion, test, and emulation experts, means even faster deployment times. Selection, implementation, and characterization/ validation testing of the power-stage is greatly decreased.

Traditionally, one of the most consuming parts for a systems integrator is evaluating the power delivery system prior to implementing. Understanding the AC characteristics and using that information to drive design decisions in the next stage has been difficult until now.

Using large signal analysis in time and frequency domains gives a significant improvement in system behaviour ahead of implementation. The real-life data that was previously unavailable can be used in the form of S-parameters to model and optimize performance.

Large-signal impedance analysis is particularly important in the non-linear world of power delivery as virtually all the components in a complex multiphase solution are nonlinear.

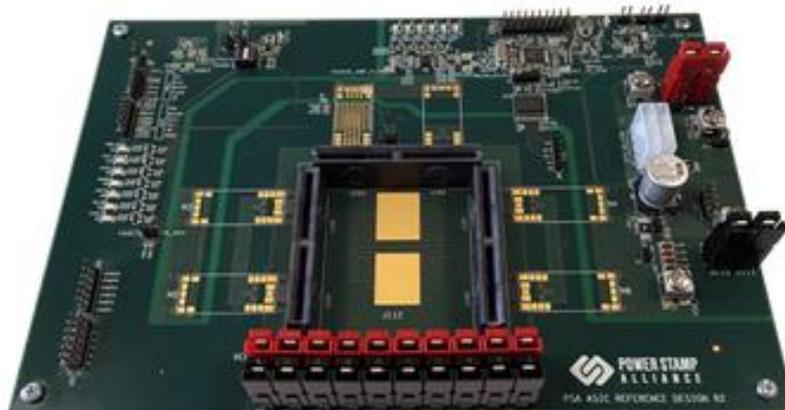
Once the power stage has been chosen, it must be characterized/validated and optimized in order to successfully use it with the target device. This process has historically taken considerable time in repeating optimize-and-test cycles.

Characterization and validation of a high current power delivery solution is very time consuming and involves three key stake holders working in tight collaboration. The power supply vendor (PSA) in this case, the digital load vendor and the systems integrator.

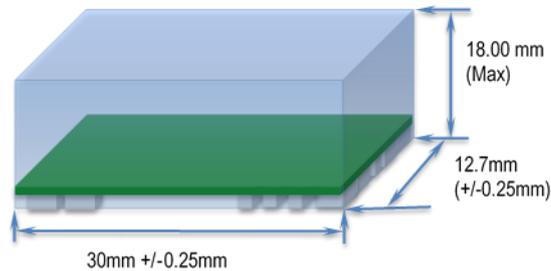
A number of studies outline the key resource allocation for getting a fully validated customer ready solution to market. The largest areas of time consumption are:

- Generating test vectors
 - Time domain
 - Frequency domain
- Measurement techniques
- Sharing and comparing information across multiple stakeholders

PSA members now can provide power-conversion and test-emulation optimized boards to accurately emulate a multitude of applications, and example of which is shown below with sockets for the load-slammers and the position for the power-stamp compliant modules to be mounted.



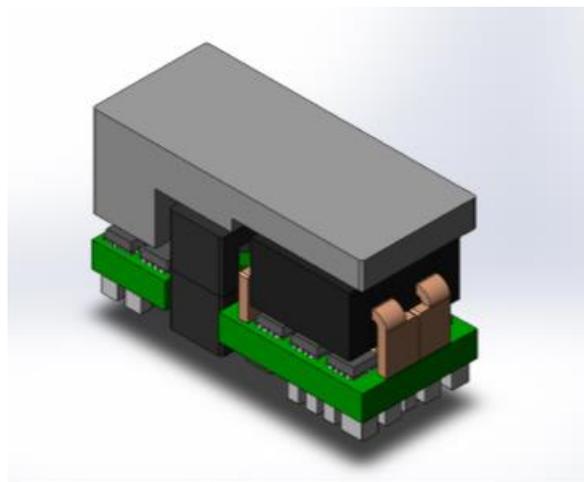
Many designers are now designing fluid-cooled applications to address the challenge of managing the dissipated heat within their applications.



**Figure 1 The Power Stamp defined envelope of
30mm X 12.7mm X 18mm; J = 300A/in³**

The PSA-defined envelope for the power-conversion stamp is shown in Figure 1 above. However, a typical realization of the satellite stamp does not use the entirety of the volume to accommodate the components that build the power conversion stage. The 'empty volume' of space within the defined envelope is used to place a baseplate to assist with the bonding of a liquid-cooled baseplate.

All PSA-compliant hardware with a baseplate will still comply to the 18mm height. This means that there is a common height dimension across all hardware that can be bonded to a common fluid-cooled heatsink. Shown in figure 2 below.



**Figure 2 Typical Power Stamp
Satellite with Baseplate Option**

Heat transfer fundamentals states that there are three basic modes of transferring heat: conduction, convection, and radiation. Forced air convection is the most relied on mode of heat removal, however, in applications like the supercomputer, where usable power density can be the highest, conduction to a fluid filled cold plate has superior heat transfer

performance. It is for this reason that the PSA offers their direct conversion modules as open frame (forced air cooled) or with a baseplate (cold plate cooled).

In a typical mechanical structure for a high-density point of use module, while maintaining a footprint that meets the system level power density requirements, it is not feasible to have direct thermal interface of all the dissipative components to the baseplate. A well-thought-out solution takes advantage of the multi-dimensional thermal interfaces using the cold plate supplemented by removing some of the heat through the connections to the host PCB via the power planes.

Using Finite Element Method (FEM) simulation tools creates a way to understand the net results of the combined structural elements. The results of such simulations (in the following Figures 3 and 4) validates the feasibility of a baseplate cooling solution in lieu of a forced air solution.

Forced Convection Simulation

The first simulation evaluates the module converting 54V to 1.8V at 70A. The unit was mounted to a PCB set at an application representative temperature with 8 layers of 3-ounce copper on planes large enough to support 70A of current. 600LFM was forced over the unit in the transverse direction. In this environment, simulations showed that a heatsink was also needed. The overall module height at 25.4mm. Fin design used 13 X 1.2mm. Air temperature for below simulation is 40°C

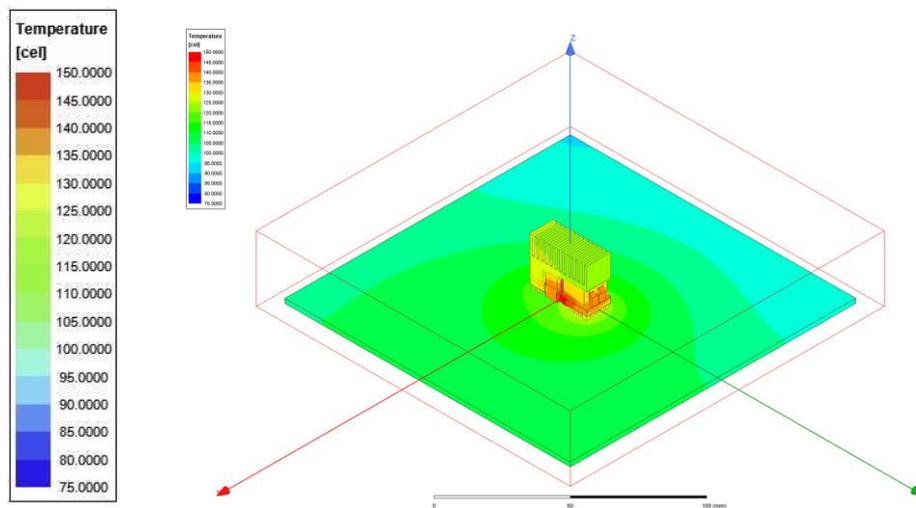


Figure 3. Full Load (70A)
Board size 100mm*100mm

Cold Plate Simulation

The second simulation evaluates the module converting 54V to 1.8V at 70A. The unit was mounted to a PCB **again set at an application representative temperature** with eight layers of 3-ounce copper on planes large enough to support 70A of current. The module's baseplate was thermally coupled to a cold plate held at 40°C.

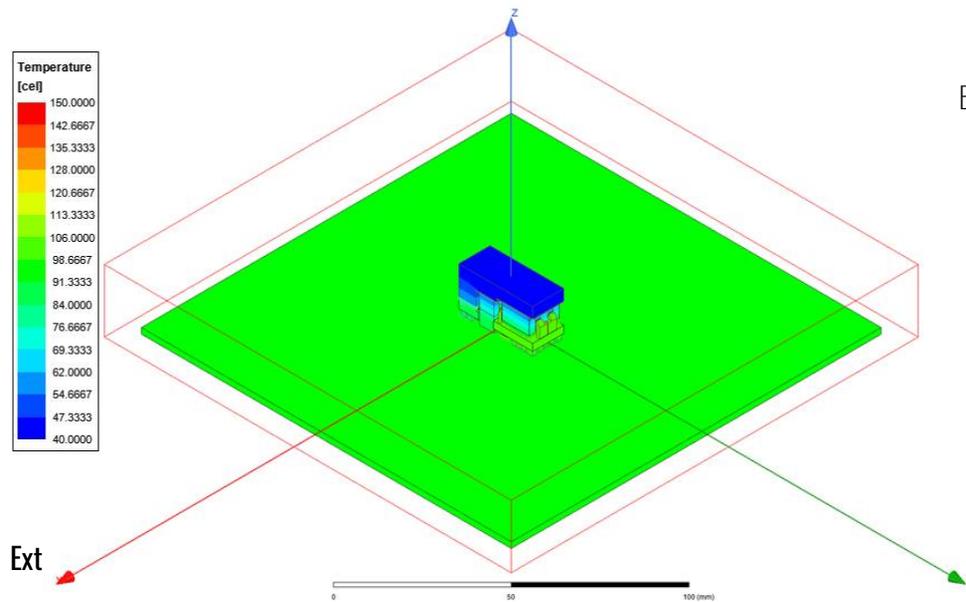
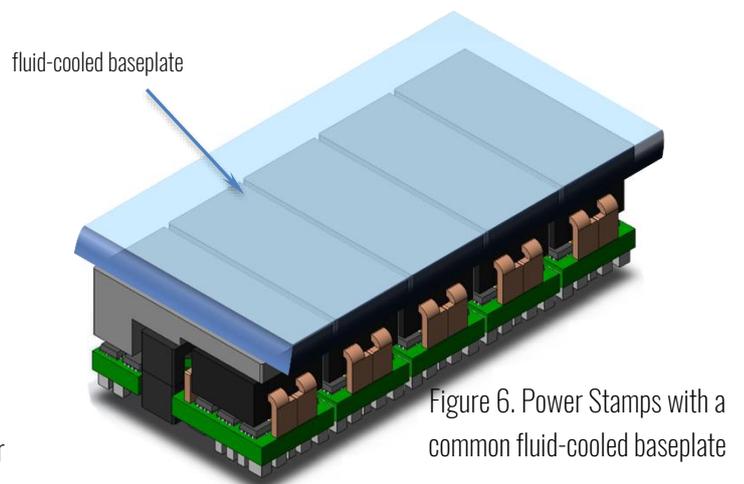
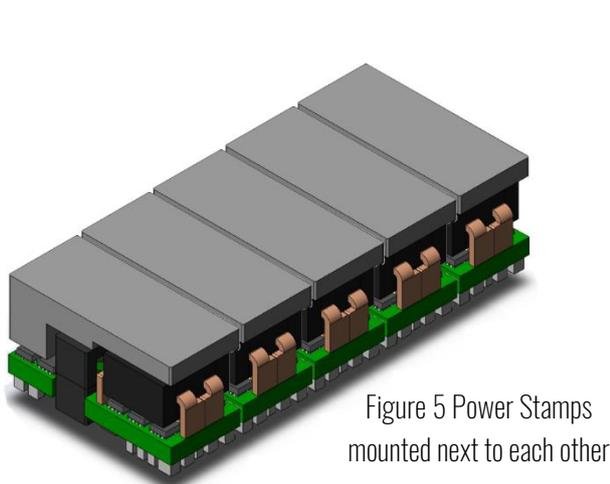


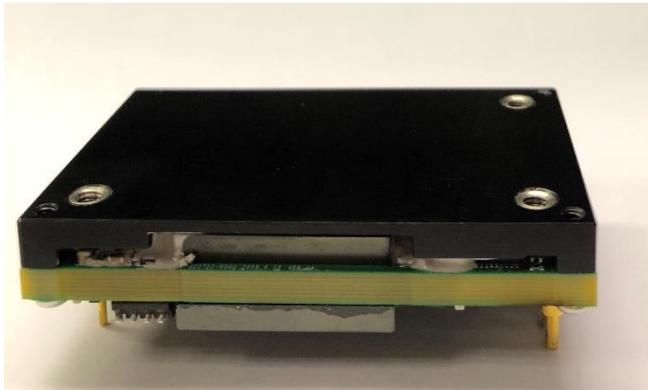
Figure 4. Full Load (70A)
Board size 100mm*100mm



Many implementations that use PSA-compliant hardware need more than one stamp to create the power stage solution required for the CPU or ASIC demand. By implementing a baseplate to the units, they will have a common surface available to be thermally bonded to a fluid cooled baseplate

Beyond this – when thinking back to the 2-stage design approach, yes, many standard 48V input ‘bricks’ do have a baseplate to thermally bond a heatsink to. (example shown below), however, the 12V input non-isolated stage does have an inherent issue of thermally bonding to a water cooled heatsink as it is very usual for that power-conversion stage to be realized from discretely mounted components. A successful implementation of a watercooled design cooling discrete components is something that must be closely managed at component level.

Example of a 48V to 12V DCDC converter with a baseplate



Conclusions

As with any thermal simulation, bench testing should be completed in the actual application to confirm results. In both forced air and cold plate applications, heat does exit the module via the PCB. It is worth mentioning that in forced air applications, the PCB can be cooled by the moving air however in the cold plate applications, only the module’s baseplate is cooled.

In most configurations, especially those where modules are paralleled and aligned close to each other, special attention should be given to the PCB temperature rise.

The anticipated method of construction of the power-stamps in the application is that they are soldered in place, then the thermal-management components integrated afterwards with high performance thermal interface materials used in the construction with the objective of minimizing thermal resistance from the module to the fluid-cooled heatsink.

A PCB layout designed with consideration of the modules in parallel and the correct manufacturing methods and processes to apply the thermal management components to them is required. By taking these steps, the power stamps themselves, the CPU losses and cooling of the main PCB can be achieved by using the design approach of a fluid-cooled cold plate.

This study shows the successful realization of a product application that benefits from the increase in power-conversion density (approx 40% reduction in overall space needed) when compared to the traditional 2-stage power conversion approach and functionality that PSA compliant units brings to 48Vin applications

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